The H2M Pixel Sensor Prototype: Laboratory Characterization

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HELMHOLTZ

DESY.

MAPS for Future Lepton Colliders

Future Lepton Colliders

- Various existing proposals: CEPC, FCC-ee, CLIC, ILC, etc.
- Challenging requirements for tracking and vertex detectors:

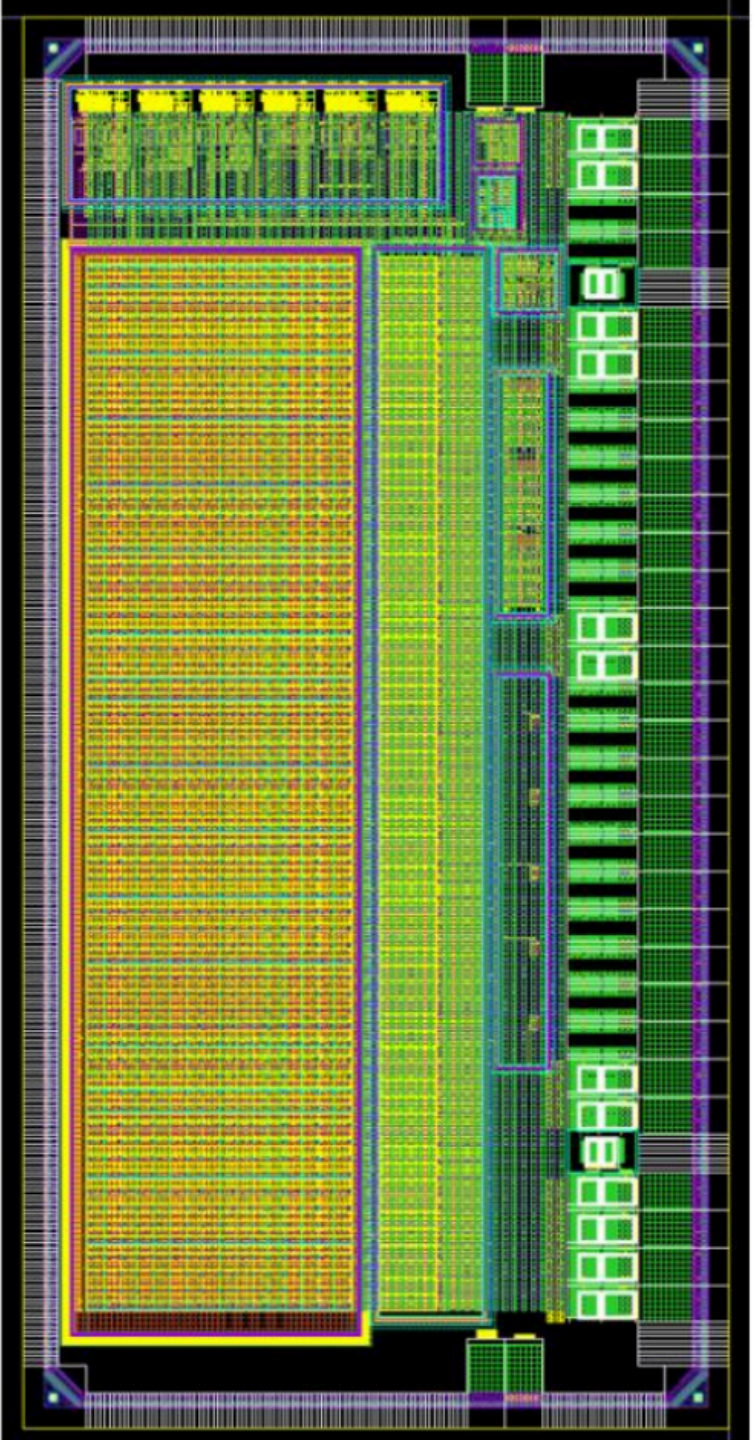
CLIC	Vertex Detector
Timing Resolution	~ 5 ns
Spatial Resolution	< 3 μm
Mass Constraint	~ 0.2%X_0
Power Dissipation	< 50 mW/cm^2
Hit Detection Efficiency	> 99.5%

K. Dort et al. doi:10.22323/1.390.0836

Monolithic Active Pixel Sensors (MAPS)

- Single sensor and fully integrated readout electronics
- Thinner devices with less multiple Coulomb scattering
- Small collection electrodes: low sensor capacitance beneficial to SNR
- Smaller feature size (e.g. 65 nm): higher density of logical circuits

↪ See talks by L. Mendes, M.A. del Rio Viera and poster by S. Ruiz Daza



The H2M (Hybrid-to-Monolithic) Prototype

H2M Pixel Sensor Prototype

Common design and testing effort between

Development goals

- Study challenges of porting a known hybrid pixel detector architecture in a monolithic chip
- Exercise digital-on-top design flow and methodology in monolithic process
- Design and test a compact digital cell library

Existing prototypes

- Designed and fabricated in 65 nm CMOS imaging process
- Currently 5 samples under investigation

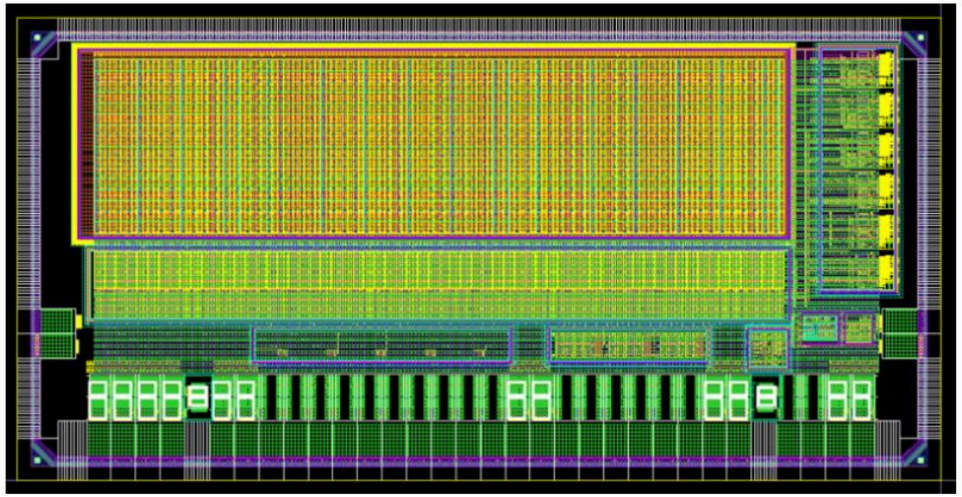
H2M Pixel Sensor Prototype

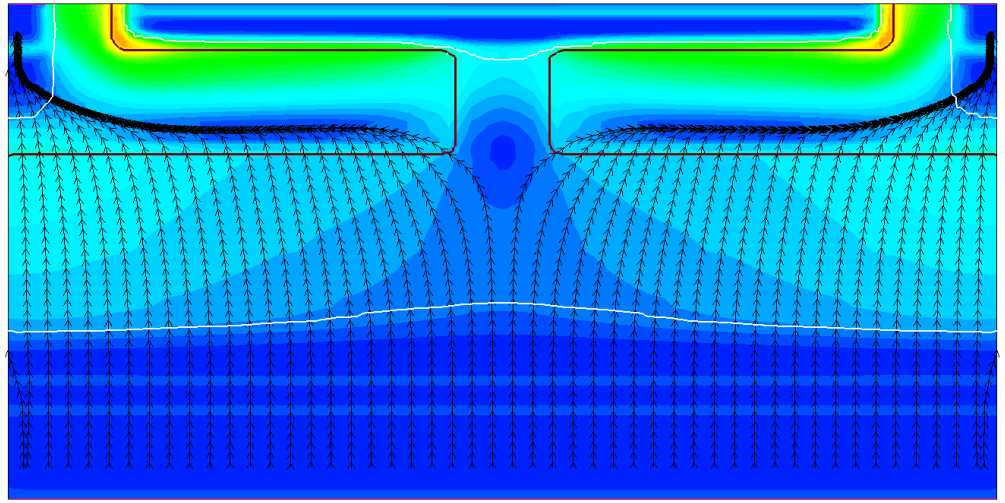
Sensor specifications

- Pixel matrix: 64 × 16 pixels
- Pixel pitch: 35 × 35 μm^2
- Total sensitive area: 2.24 × 0.56 mm^2
- Relatively thin epitaxial layer: 10 µm
- Total thickness: 50 µm

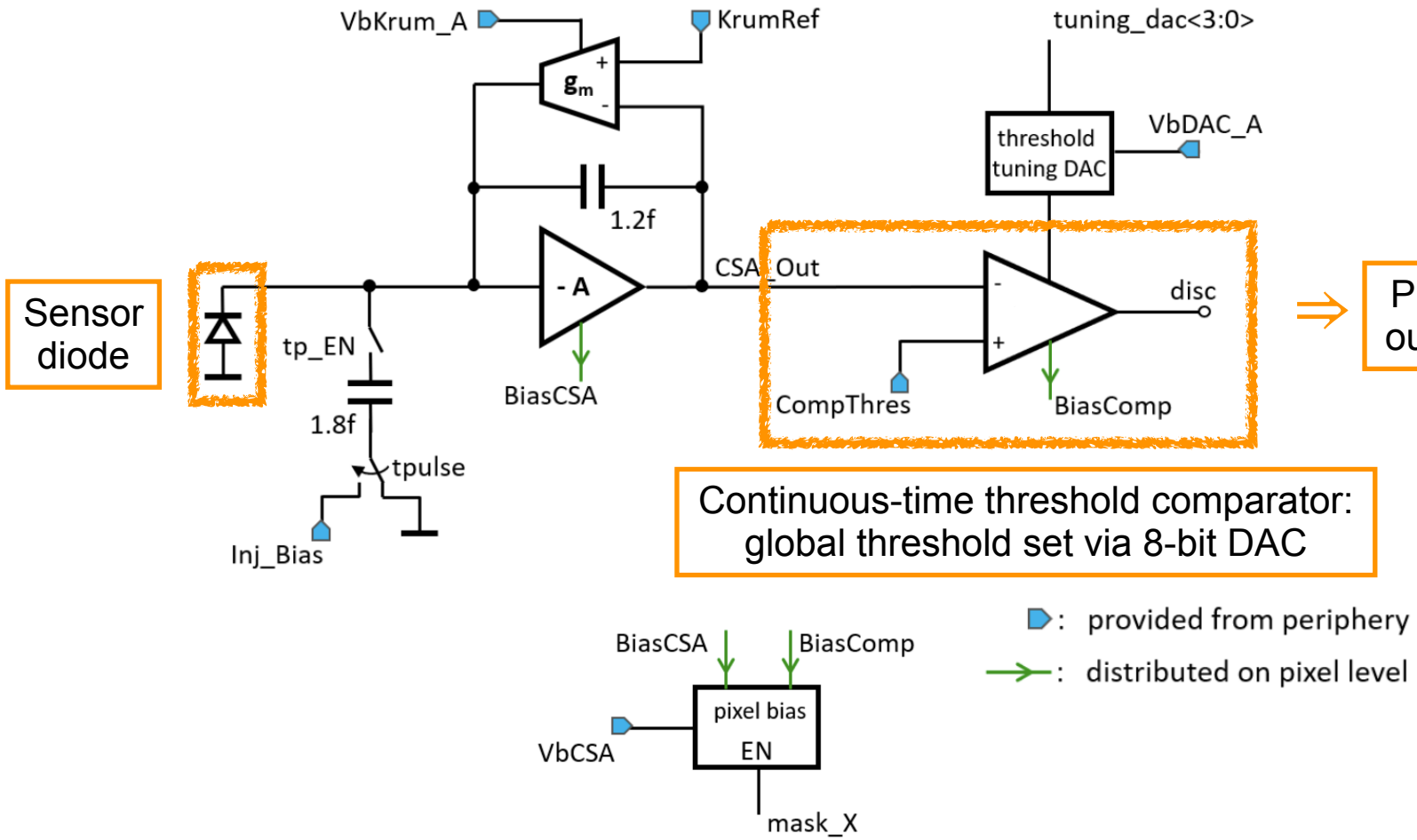
N-gap sensor layout

- Additional n-doped layer with gaps around pixel edges
- 2.5 µm gap size
- Improve charge collection from pixel edges and corners





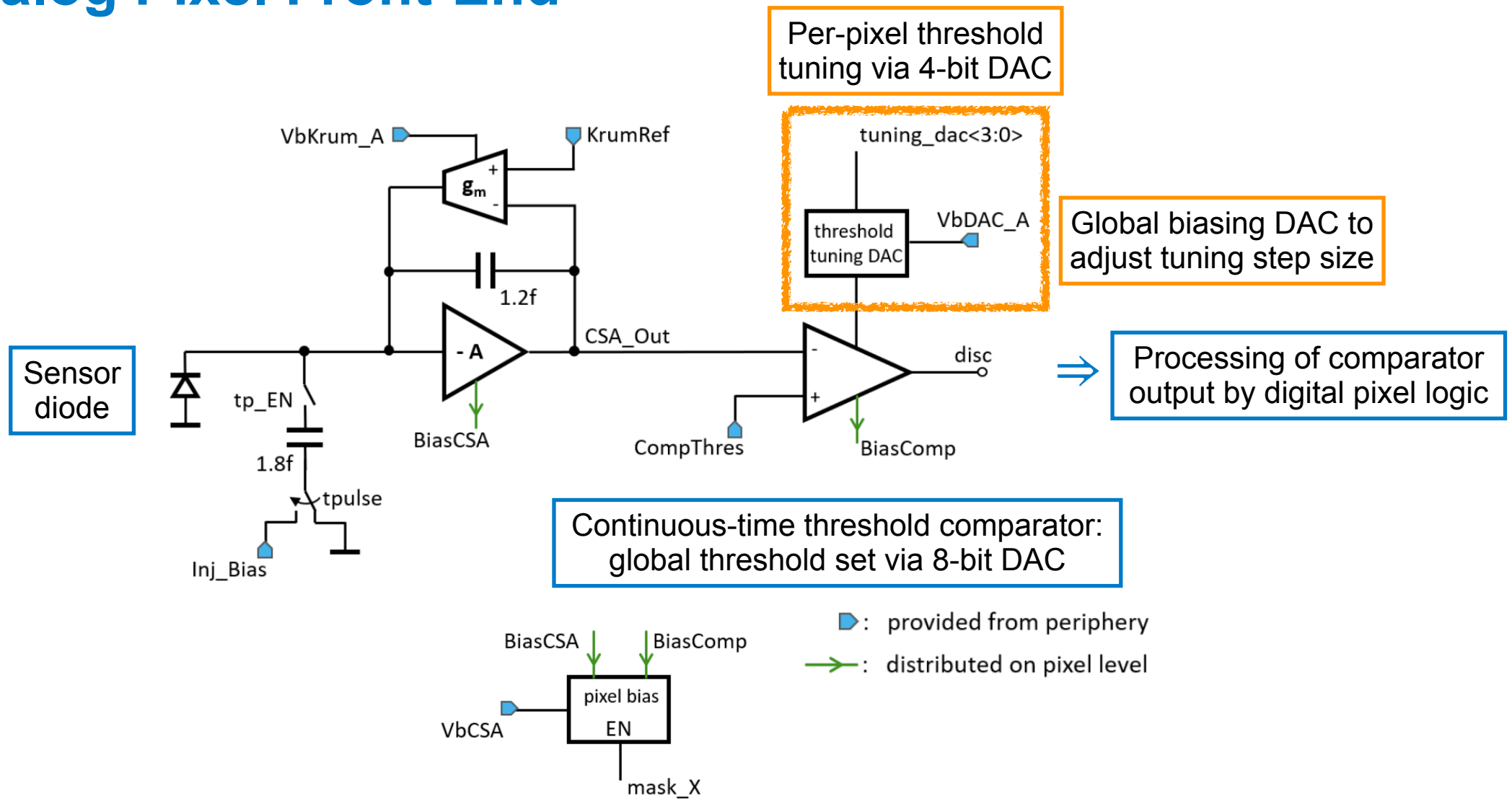
Analog Pixel Front-End



⇒ Processing of comparator output by digital pixel logic

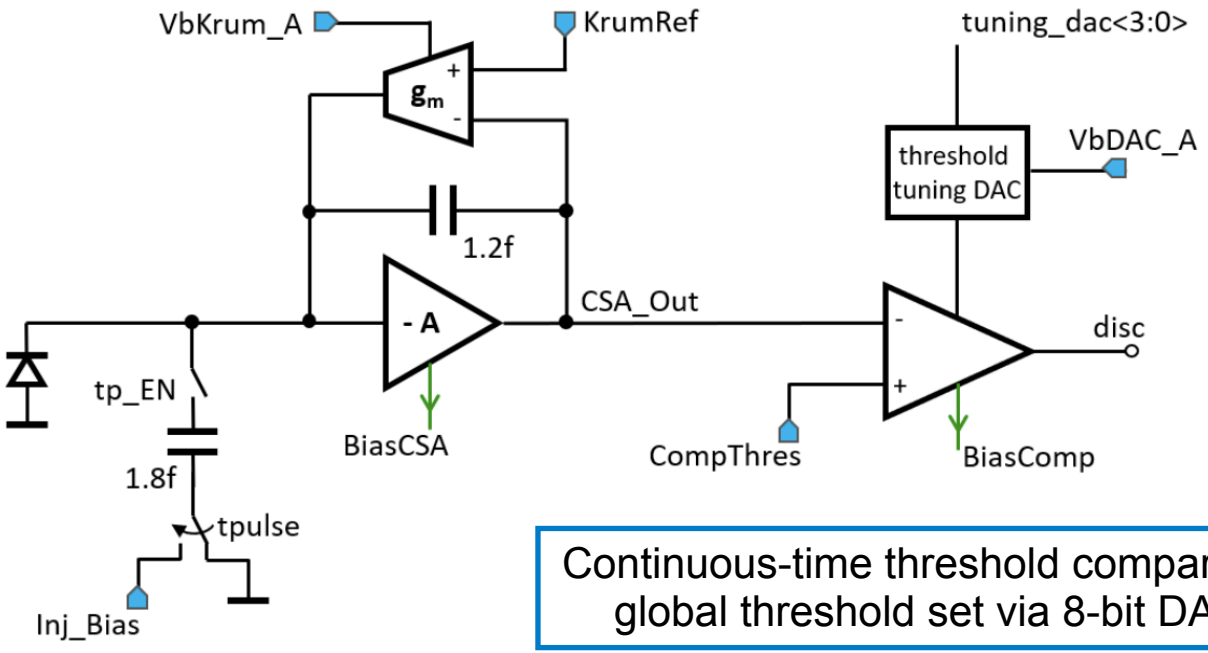
Continuous-time threshold comparator: global threshold set via 8-bit DAC

Analog Pixel Front-End



Analog Pixel Front-End

Per-pixel threshold tuning via 4-bit DAC

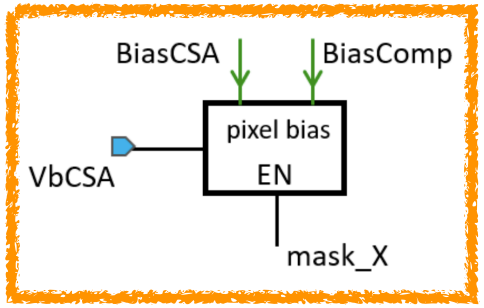


Sensor diode

Global biasing DAC to adjust tuning step size

⇒ Processing of comparator output by digital pixel logic

Continuous-time threshold comparator: global threshold set via 8-bit DAC



: provided from periphery

: distributed on pixel level

Mask bit: enable or disable pixels

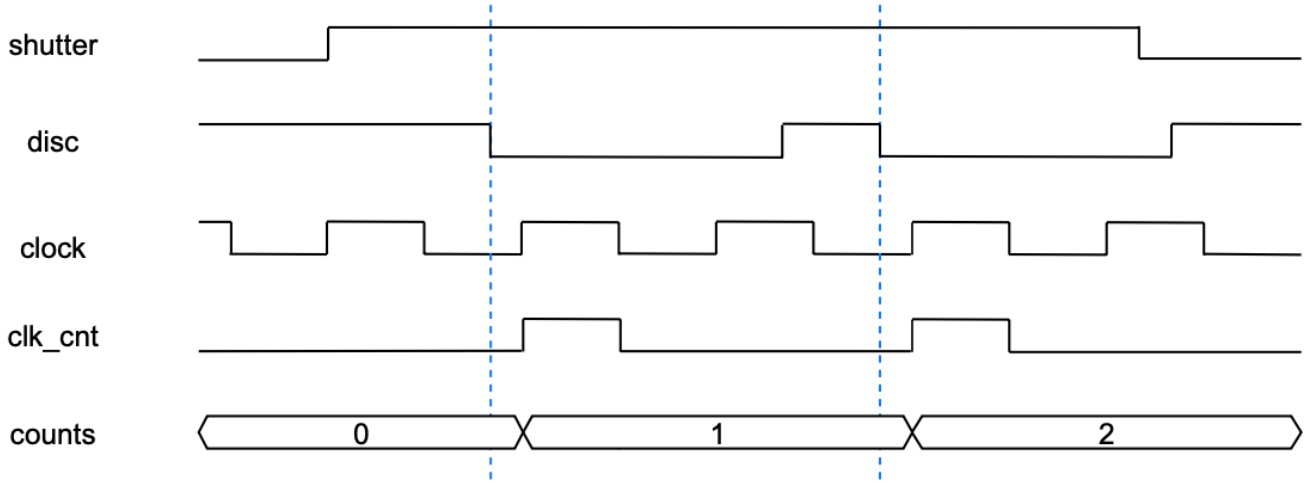
Digital Pixel Logic

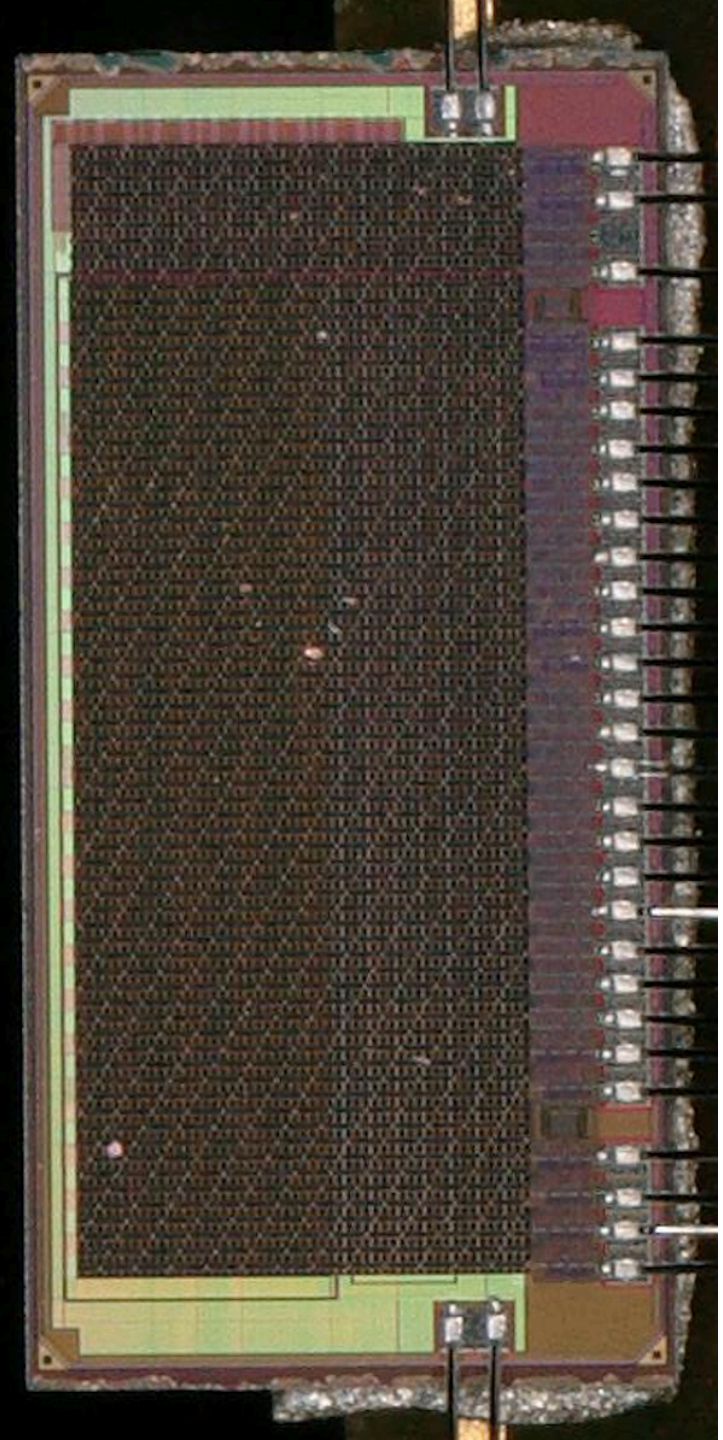
Based on 8-bit in-pixel counter with 4 different acquisition modes

- Frame-based acquisition modes
  - Active window defined by external shutter signal
  - Time of arrival (ToA)
  - Time over threshold (ToT)
  - Photon counting
- Triggered binary readout

Example: photon counting mode

- Triggering on discriminator falling edge
- 10 ns binning
- Counts number of threshold crossings (i.e. amplified signal exceeds global threshold) within shutter window





Laboratory Characterization

Noise Based Pixel Trimming

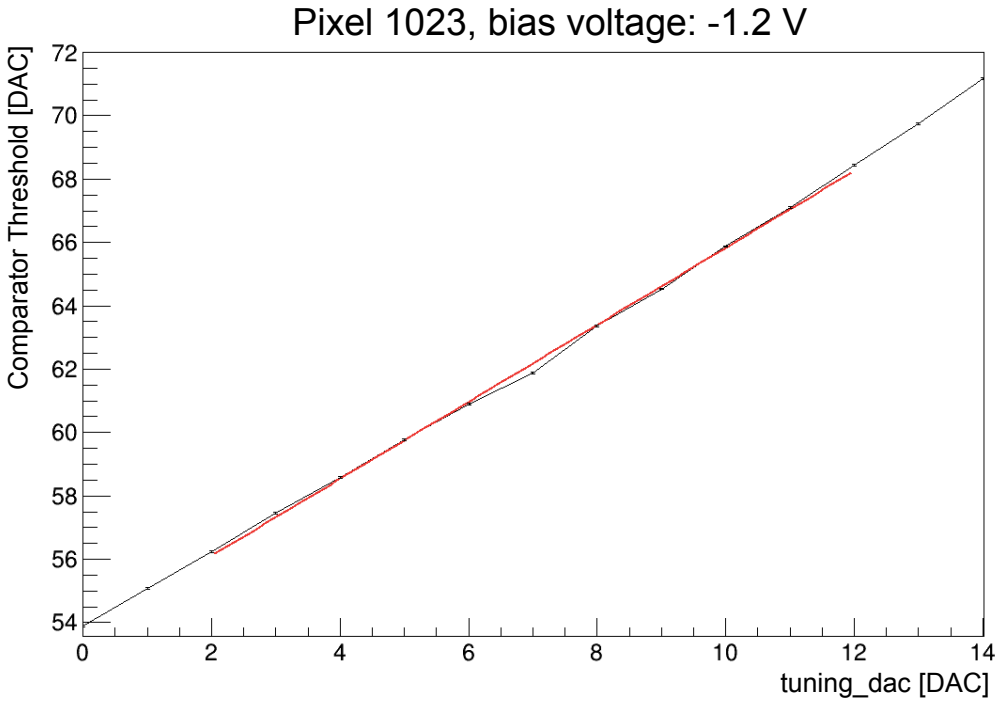
Signal detection is limited by noise effects

- Pixel baseline fluctuations
- Pixel threshold inhomogeneities

⇒ Minimize threshold dispersion of pixel matrix by means of per-pixel threshold *tuning_dac*

Procedure

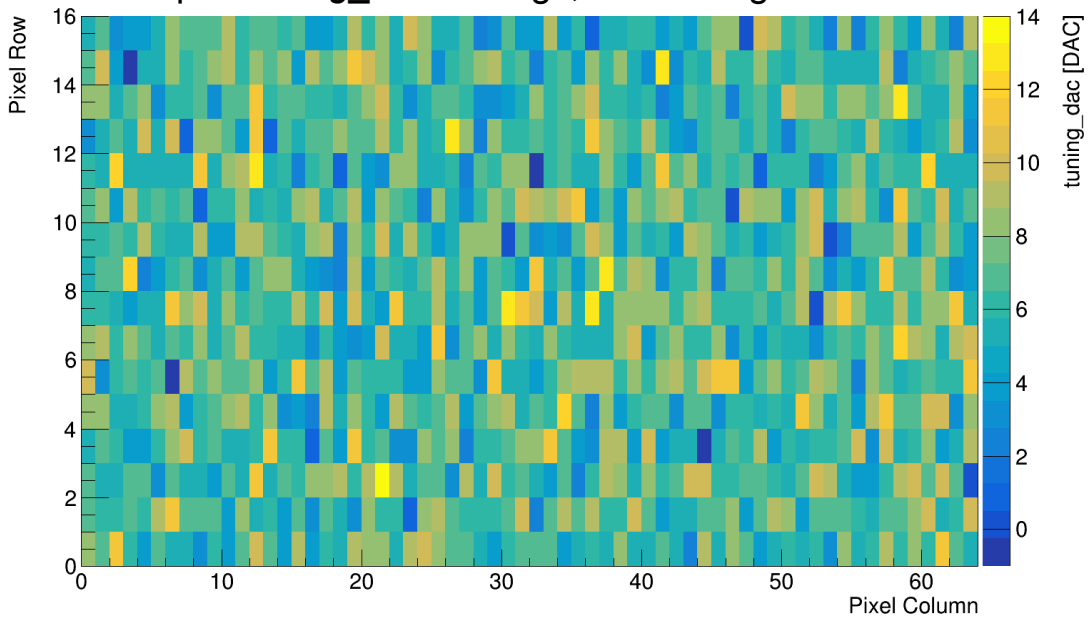
- Repeat threshold scan for all *tuning_dac* settings
- Determine individual pixel thresholds
- Choose trimming target within range of all pixels
- Find matching *tuning_dac* setting via linear fit
- Create mask file with per-pixel *tuning_dac* setting



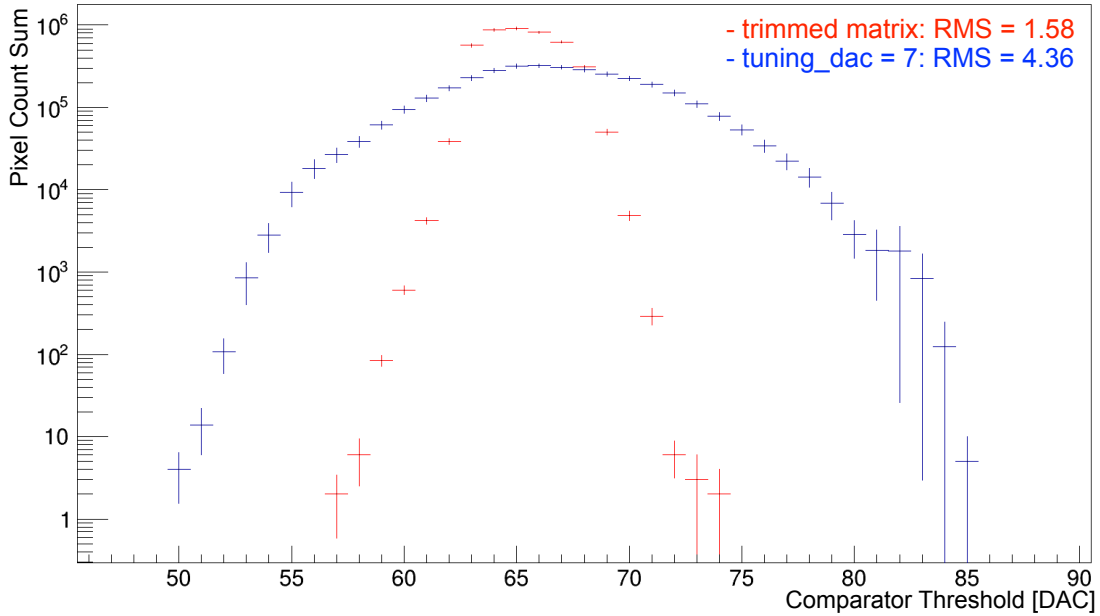
Trimmed Pixel Matrix

- Reduced threshold dispersion
- No trends in map of *tuning_dac* distribution
- Threshold *tuning_dac* makes use of full dynamic range
- Approximately 0.5 % of the pixels not tuneable

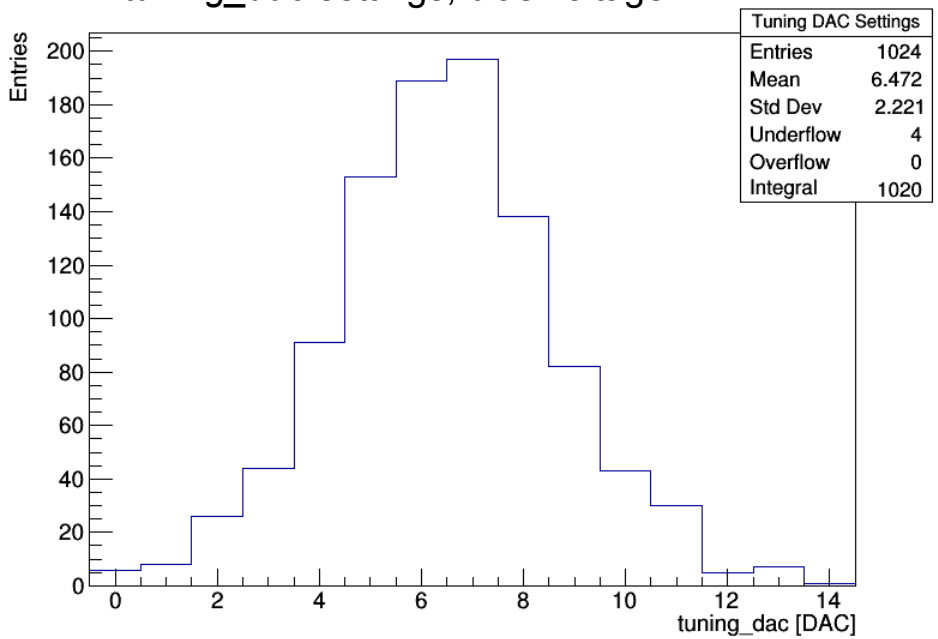
Map of *tuning_dac* settings, bias voltage: -1.2 V



Pixel count sum (whole matrix), bias voltage: -1.2 V



tuning_dac settings, bias voltage: -1.2 V



Front-End Parameter Optimization

8-bit global biasing *dac_itrim*

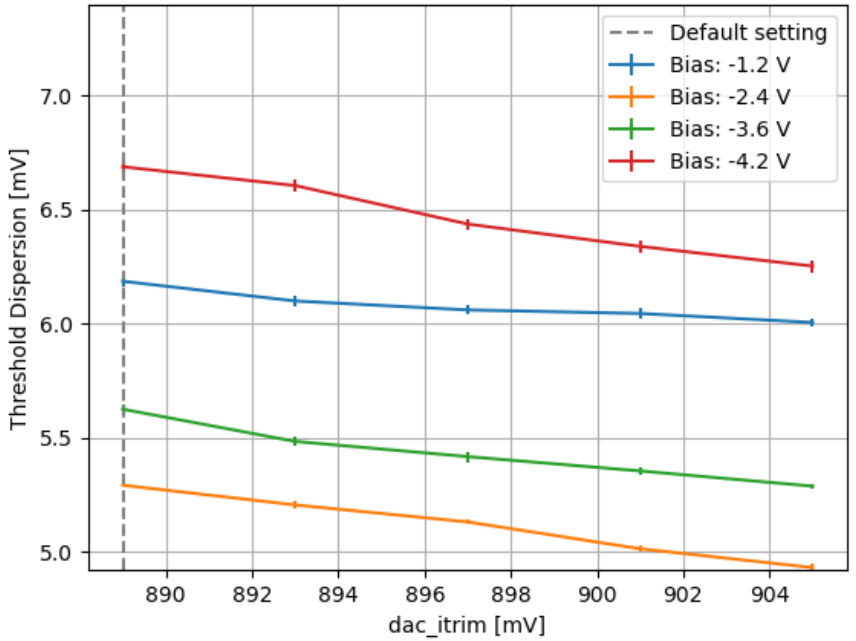
- Varies bias voltage of threshold *tuning_dac* to adjust tuning step size

  ⇒ affects dynamic range of *tuning_dac*, amount of tuneable pixels and threshold dispersion
- Compromise between low threshold dispersion and high amount of tuneable pixels
- Choose operation point for different bias voltages based on these results

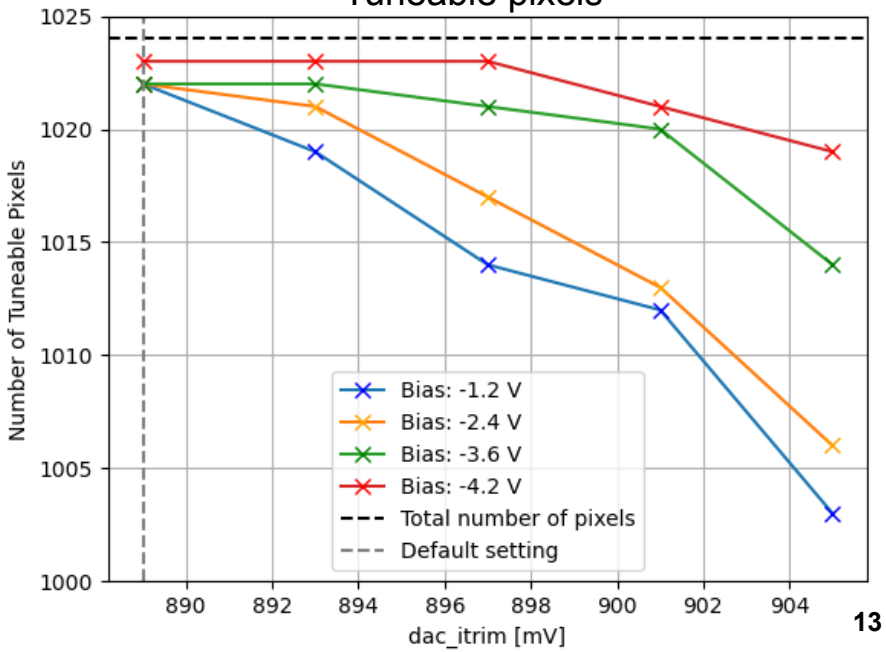
  ⇒ already reasonable operation point at default settings

  ⇒ settings might require changes in the future e.g. for different samples

Threshold dispersion

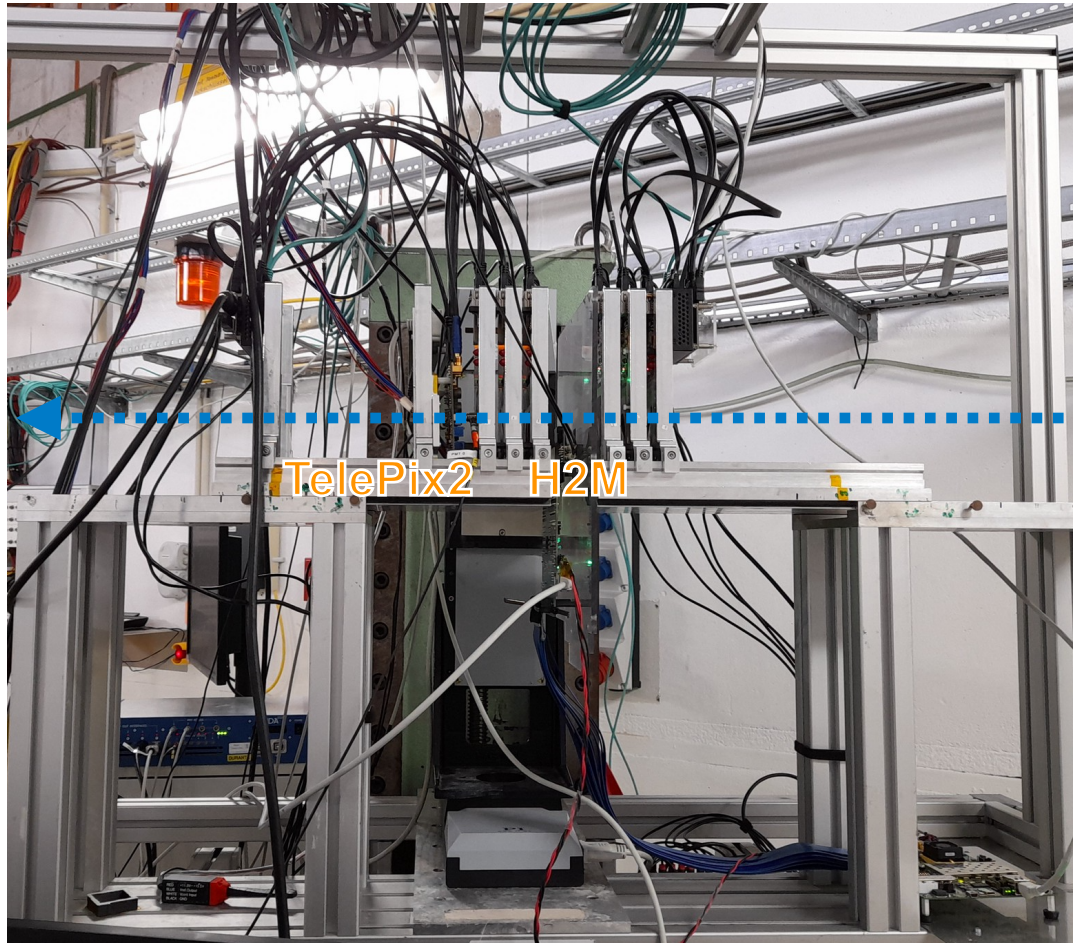


Tuneable pixels



Test Beam Operation @ DESY II

Test Beam Operation



DESY II test beam facility

↪ See talk by R. Diener et al.

- Beamline 22
- ~ 5.0 GeV electron beam
- ALPIDE reference telescope with ~ 3 µm pointing resolution

↪ See talk by A. Herkert

- Trigger: TelePix2

↪ See poster by A. Wintle

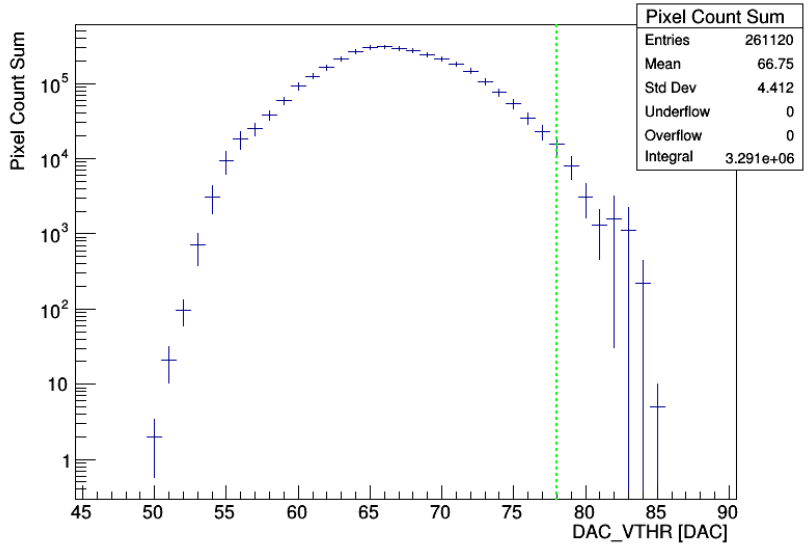
- H2M: ToA mode

Untrimmed Pixel Matrix

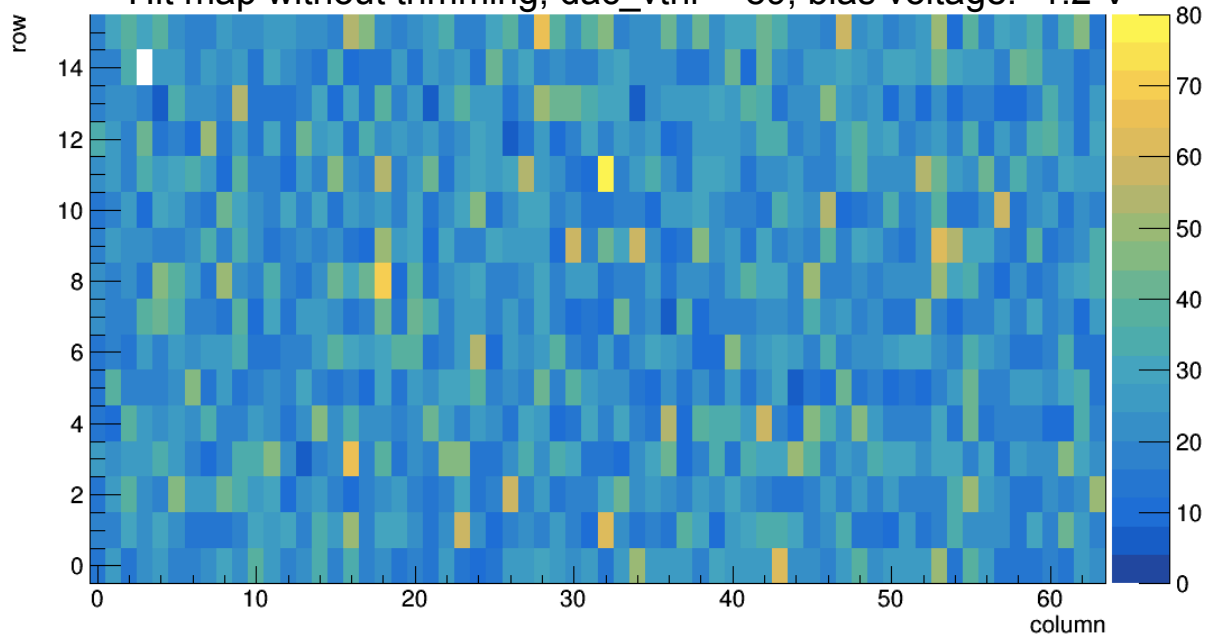
Hit maps

- Comparably homogeneous but also noisy pixels for high hit detection thresholds
- Noise dominated and non-operational for reduced hit detection thresholds

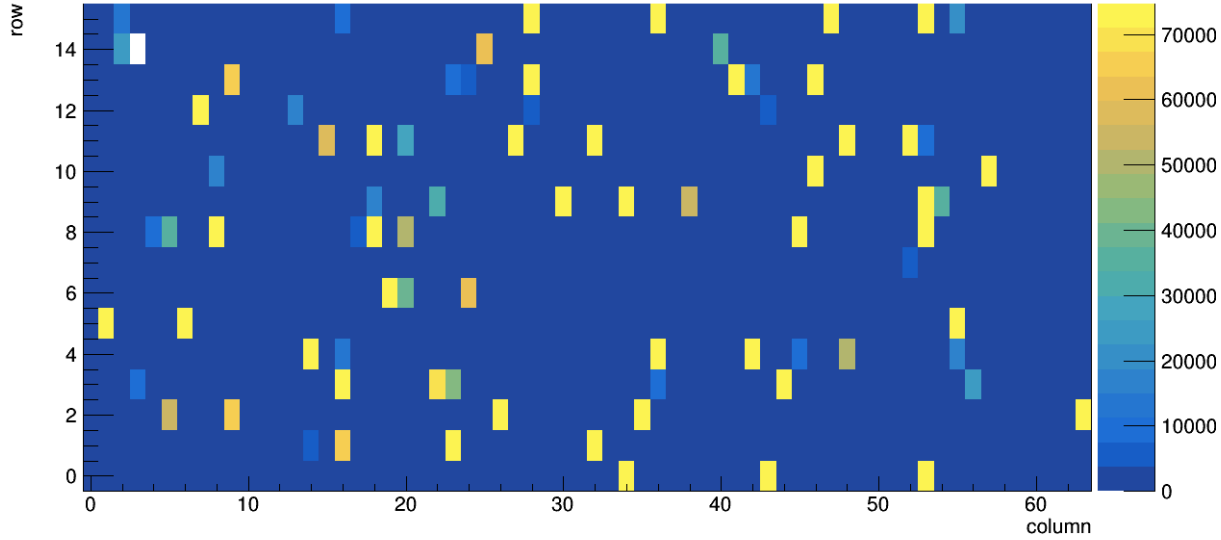
Pixel count sum (untrimmed), bias voltage: -1.2 V



Hit map without trimming, dac_vthr = 89, bias voltage: -1.2 V



Hit map without trimming, dac_vthr = 78, bias voltage: -1.2 V



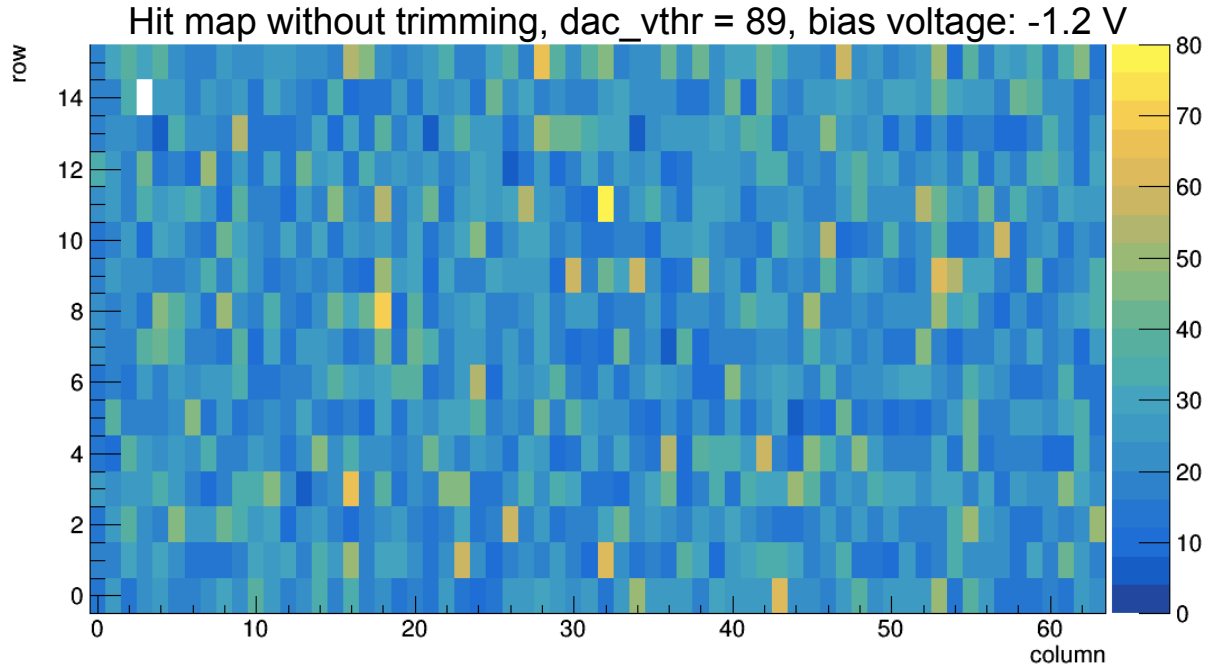
Hit Maps

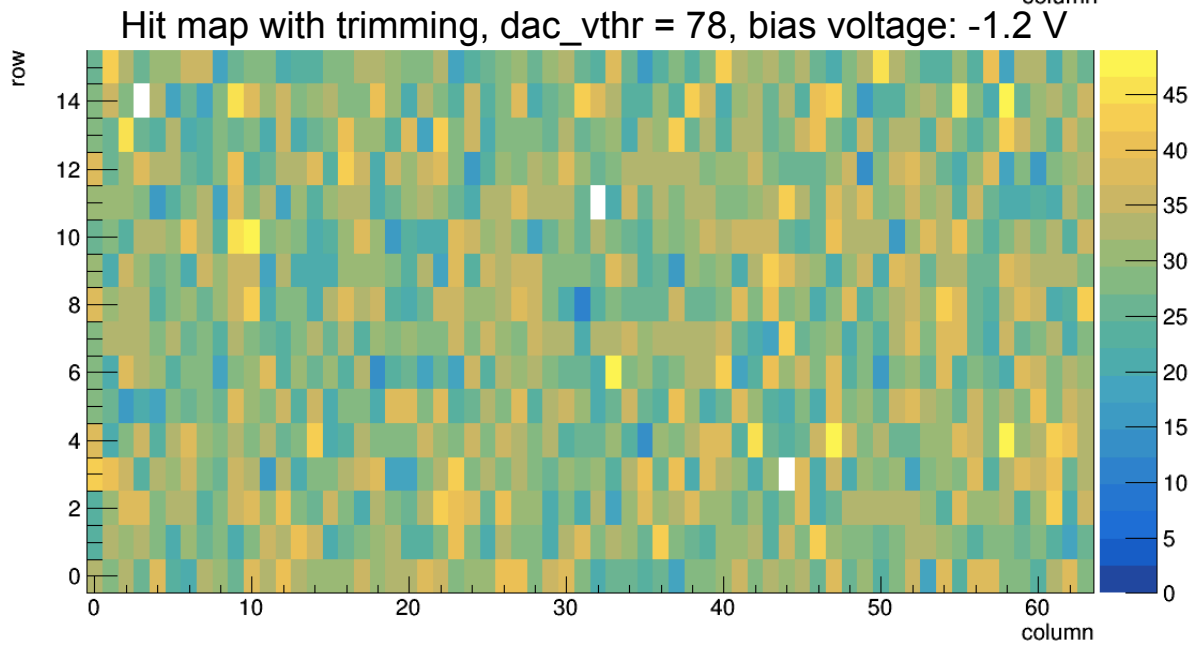
Trimmed and untrimmed pixel matrix

- Hit detection threshold set well above individual pixel thresholds
- Comparable fake hit rate

Trimmed matrix

- Masking of three non-tuneable pixels during trimming procedure
- Homogeneous distribution
- Fully functional at lower hit detection threshold compared to untrimmed matrix





Summary & Outlook

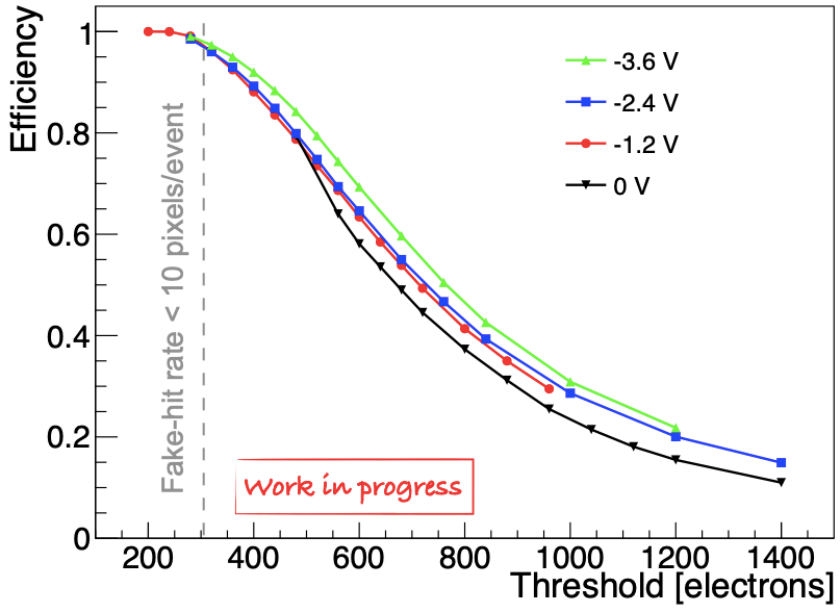
Summary

- Full hybrid design ported into monolithic chip in 65 nm CMOS imaging process
- Successful first laboratory measurements
  - Implementation of noise based trimming procedure
  - Optimization of trimming procedure by means of global *dac_itrim*
  - Pixel threshold trimming already in desired range at default settings
- Chip features work as intended
- Test beam operation @ DESY II and SPS

↪ See poster by S. Ruiz Daza

Outlook

- In-depth studies of different H2M prototypes
- Charge calibration for the test beam characterization of the samples



Thank you!

Contact

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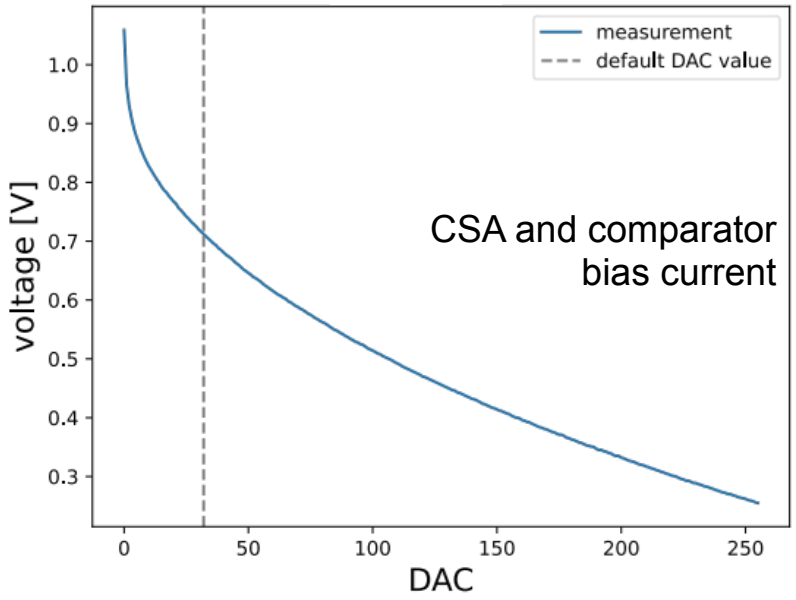
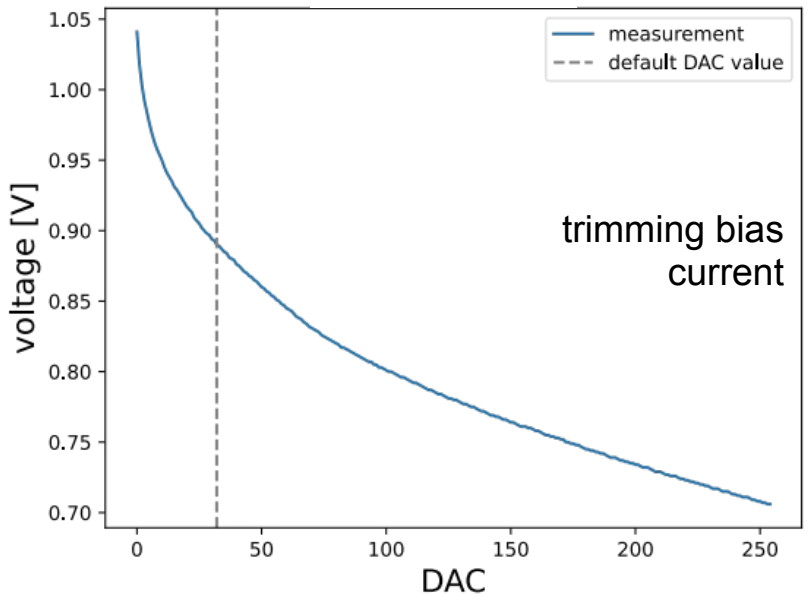
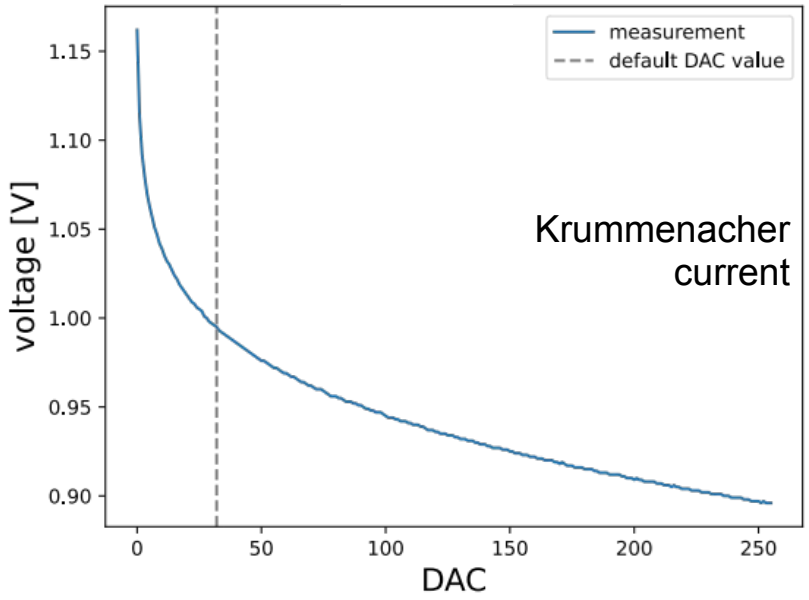
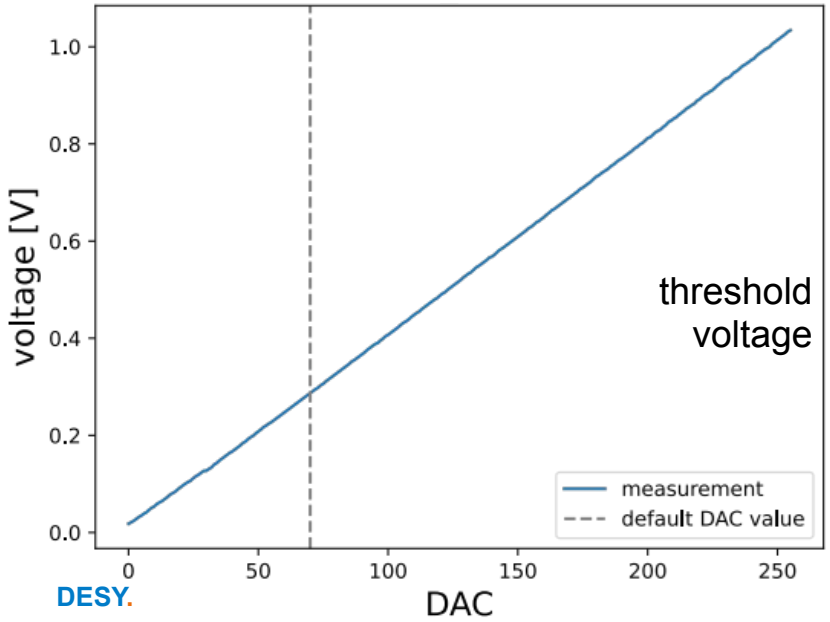
Backup Slides

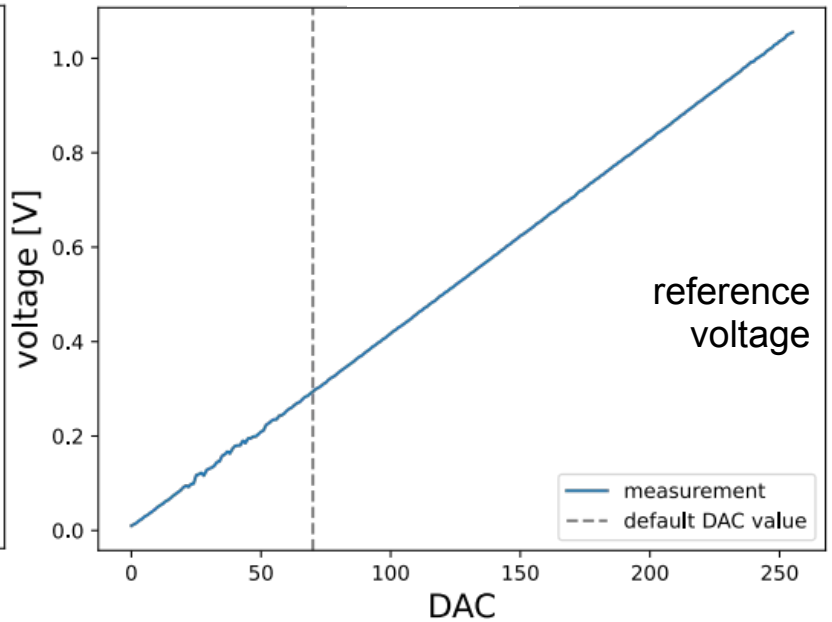
DAC Scans - Expected Behaviour Observed

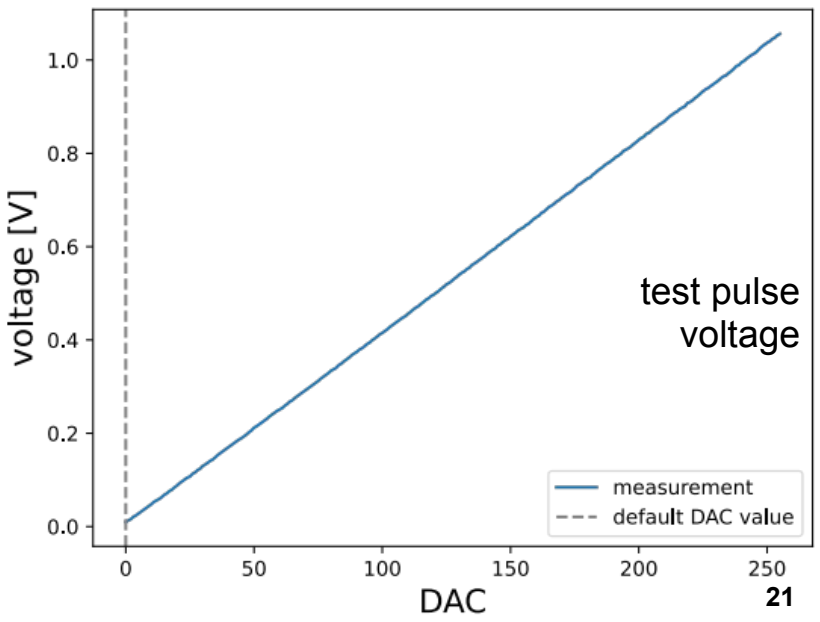












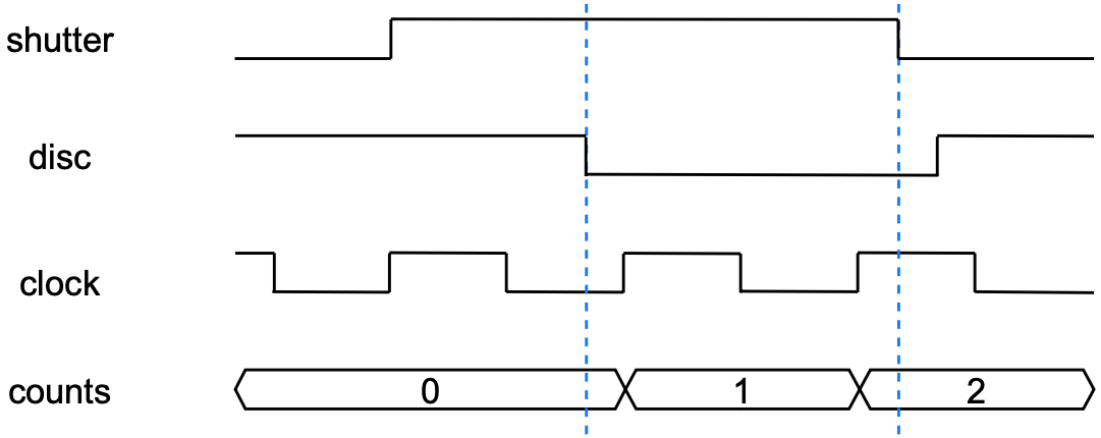
Frame-based Acquisition Modes

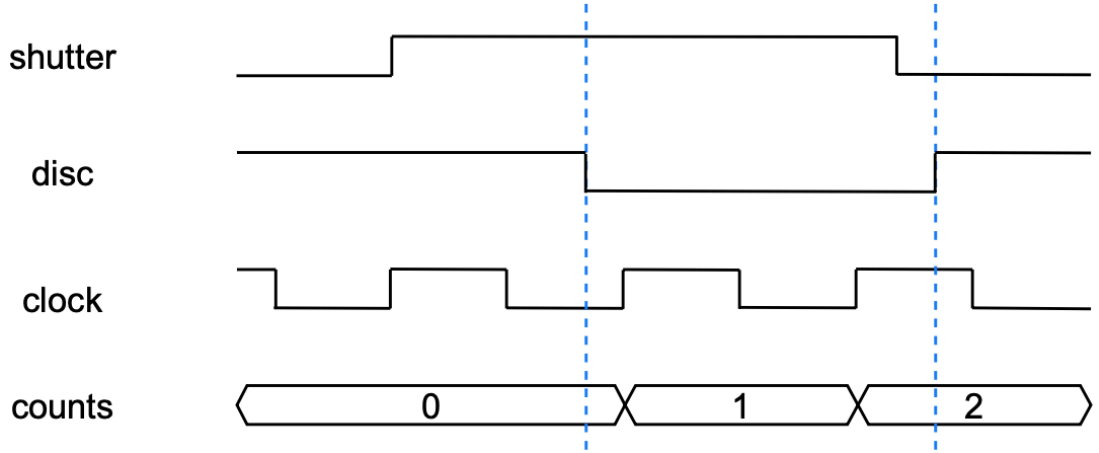
Time-of-arrival (ToA)

- Triggering on discriminator falling edge
- Counts number of acquisition clock cycles (duration of 10 ns) until shutter window closes
- End of shutter window set via external trigger signal

Time-over-threshold (ToT)

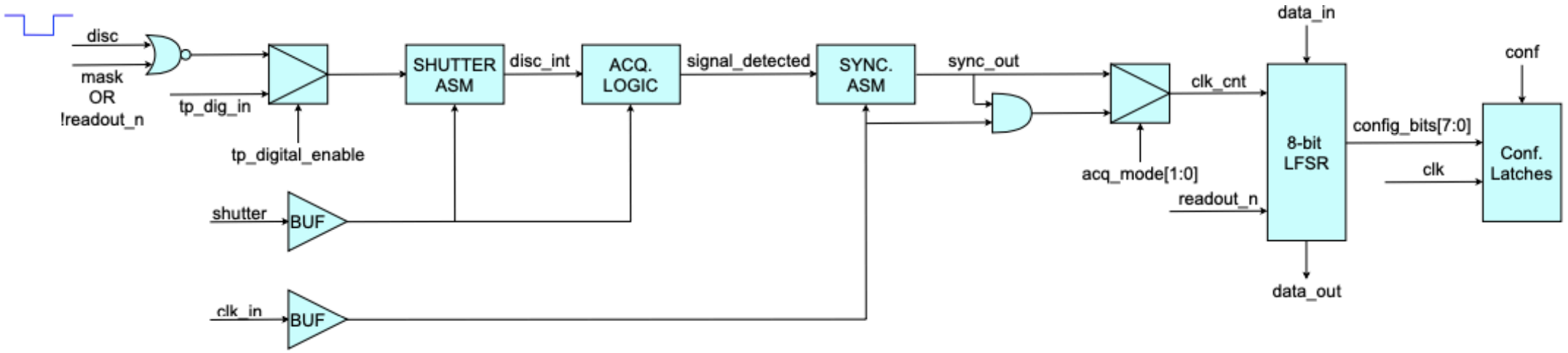
- Triggering on discriminator falling edge
- Counts number of acquisition clock cycles until discriminator signal rising edge (even after shutter window closes)
- ToT ~ collected charge (after calibration)





Pixel Digital Logic: Frame-based Acquisition Modes

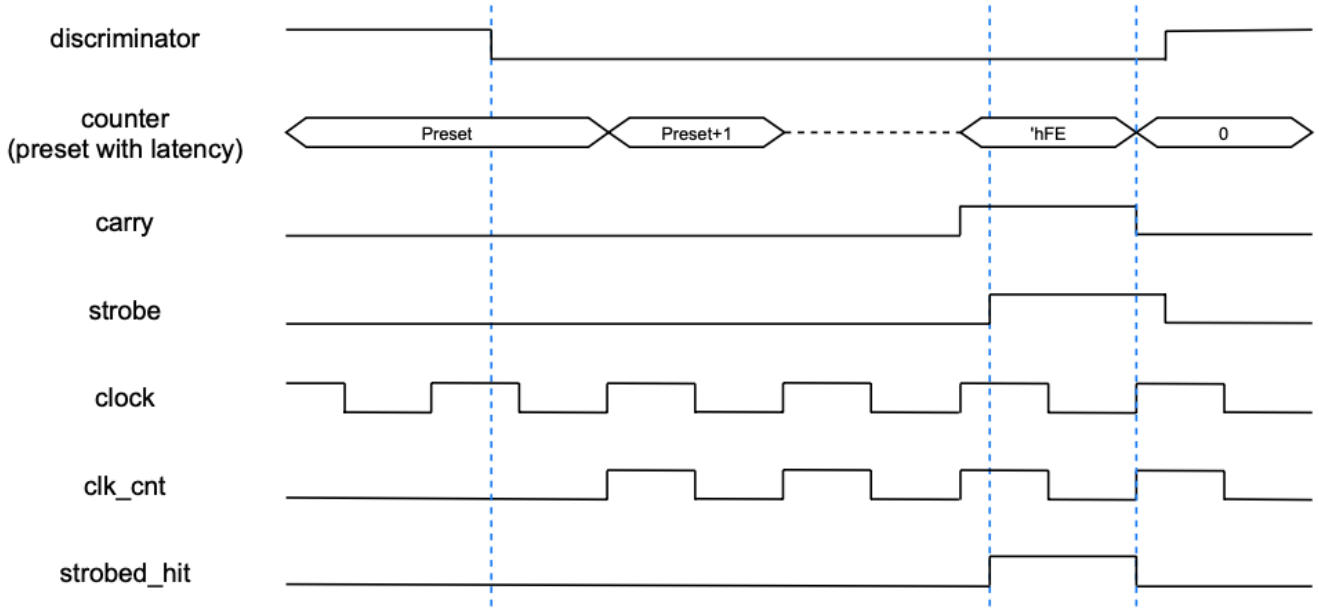
- Discriminator output: readout or masking
- Digital test pulses: enabling overwrites discriminator output
- Shutter asynchronous state machine (ASM): discards trigger outside of shutter window
- Acquisition logic (ACQ. LOGIC): produces signal based on used acquisition mode
- Synchronising logic (SYNC. ASM): synchronises signal to acquisition clock
- Counting → data stored in 8-bit linear-feedback shift register (LFSR); 8-bits for pixel configuration
  - Readout: 8-bits shifted from top to bottom of column
  - Configuration: 8-bits shifted from bottom to top of column and set to pixels



Triggered Binary Readout

- Counter preset with trigger latency value
- Triggering on discriminator falling edge

  ⇒ starts counter at preset value
- Carry signal produced as soon as counting reaches overflow
- External strobe signal provided, synchronised with acquisition clock
- Hit: carry and strobe signal in coincidence
- Variable configuration: pixel stores its own hit or combines data from group of pixels

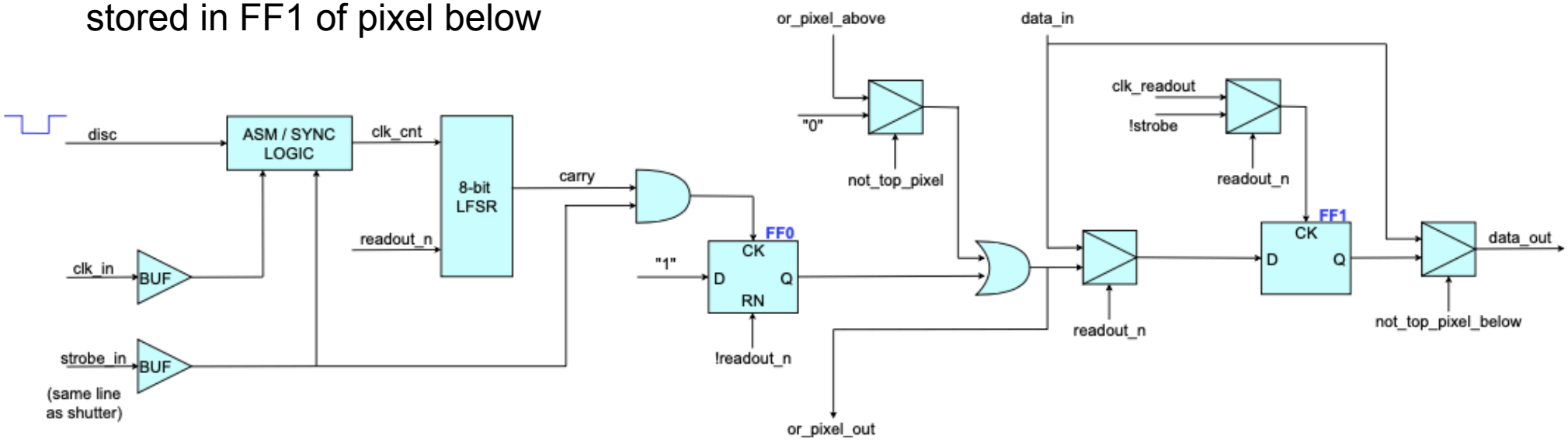


Pixel Digital Logic: Triggered Binary Readout

- External strobe signal is distributed analogously to shutter signal
- Hit when carry and strobe signal are in coincidence: flip-flop (FF0) is set

  ⇒ Result registered to flip-flop (FF1) after delay (one clock cycle after strobe signal rises)

  ⇒ Readout of FF1
- Possible to combine information of several pixels via not_top_pixel configuration of pixel below:
  - not_top_pixel = 0: hit will be stored in FF1 and read out
  - not_top_pixel = 1: FF0 is input to FF0 of pixel below; information of both pixels is ORed and result is stored in FF1 of pixel below



Tuning DAC

Mapping

- Implemented in peary
- *tuning_dac* 0: most negative comparator offset voltage
- *tuning_dac* 7: zero comparator offset voltage (no shift)
- *tuning_dac* 14: most positive comparator offset voltage

Threshold *tuning_dac* control bits for dac_itrim 82 nA

tuning_DAC				DAC#	Comp. current (nA)	Comp. offset voltage (mV)
<0>	<1>	<2>	<3>			
0	0	0	0	0	+370.6	+41
0	1	0	0	2	+318.8	+35
0	0	1	0	4	+266.4	+29
0	1	1	0	6	+213.8	+23
0	0	0	1	8	+161.0	+17
0	1	0	1	10	+107.8	+12
0	0	1	1	12	+54.3	+6
0	1	1	1	14	0	0
1	1	1	1	15	0	0
1	0	1	1	13	-54.3	-6
1	1	0	1	11	-107.8	-12
1	0	0	1	9	-161.0	-17
1	1	1	0	7	-213.8	-23
1	0	1	0	5	-266.4	-29
1	1	0	0	3	-318.8	-35
1	0	0	0	1	-370.6	-41

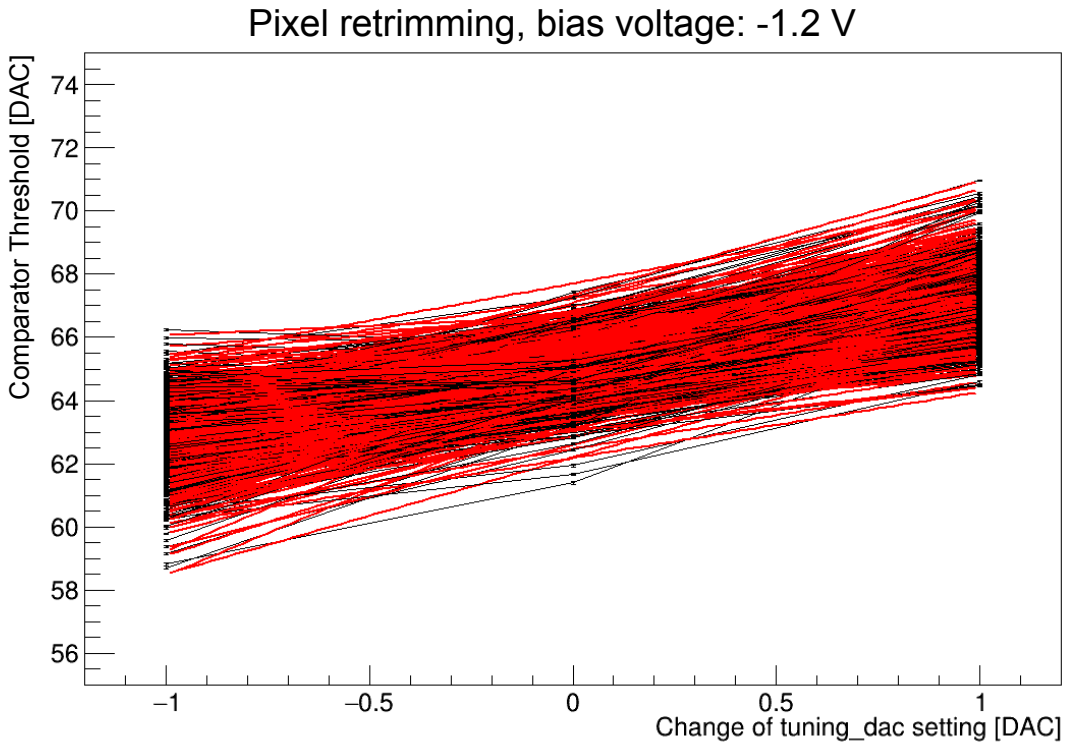
Pixel Retrimming

Re-evaluation of fractions of the matrix

- Two additional noise scans with *tuning_dac* setting above and below the initial one
- Redo linear fit in this region of interest

  ⇒ changes *tuning_dac* setting for approx. 25% of the pixels
- Retrimming only slightly reduces threshold dispersion
  - Trimming: (6.21 ± 0.02) mV
  - Retrimming: (6.17 ± 0.03) mV

  ⇒ stable voltage supply within pixel matrix



Estimation of Threshold Dispersion

- Integer *tuning_dac* settings can cause offset Δy to intended trimming target $\Rightarrow \Delta y = m \cdot \Delta x \in [0,m]$
- Estimation for whole matrix: consider average pixel slope $\bar{m}$ and statistical distribution of offset Δy

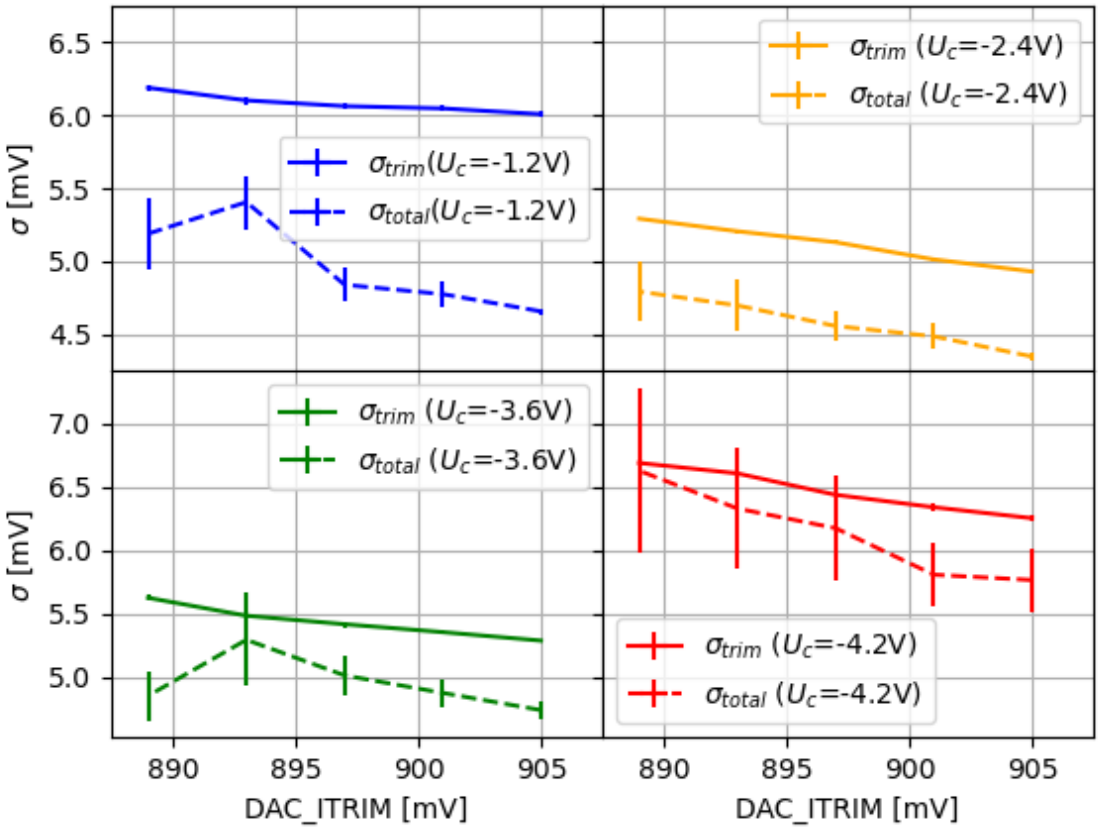
$$\Rightarrow \sigma_{\text{offset}} = \frac{\bar{m}}{\sqrt{12}}$$

- Offsets for all pixels and baseline noise contribute to threshold dispersion of whole pixel matrix

$$\Rightarrow \sigma_{\text{total}} \approx \sqrt{\sigma^2_{\text{offset}} + \sigma^2_{\text{noise}}}$$

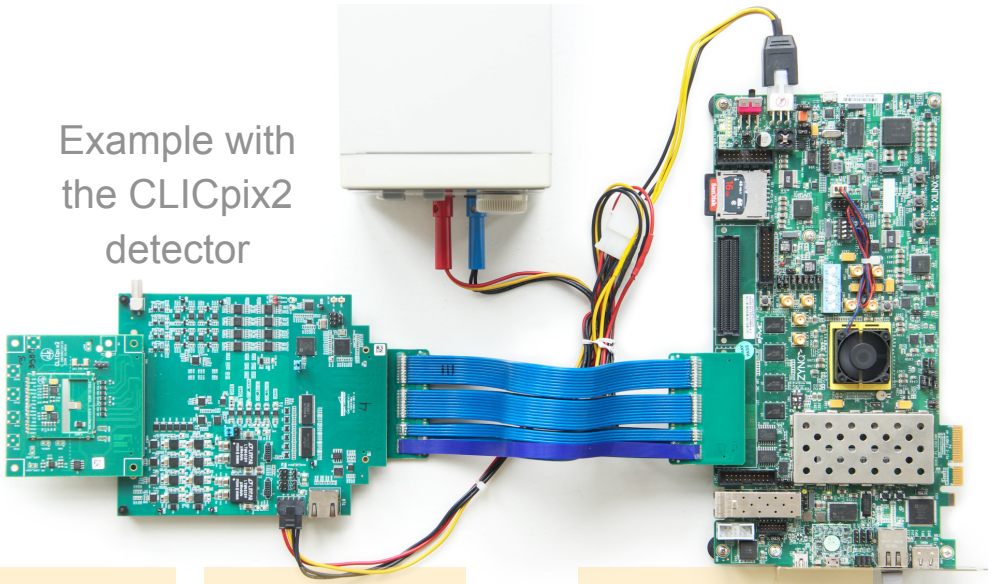
- Noise approximation σ_{noise} via averaged standard deviation of gaussian fits

Threshold dispersion



⇒ Trimming procedure results in threshold dispersion σ in desired range

Caribou Data Acquisition System



T. Vanat doi:10.22323/

➢ **Zynq-Board:**

- User connects via ssh/Ethernet
- Runs Linux system with DAQ and control software
- An FPGA runs custom hardware blocks for data processing

➢ **CaR board (Control and Readout Board):**

- Physical interface between Zynq-Board ↔ Chipboard
- Contains all peripherals needed to interface and run the chip (eg. adjustable voltage/current references, pulser control…)

➢ **Chipboard:**

- Application-specific detector carrier board
- Mostly passive components + detector chip