Test-beam results of single-event-effect studies on prototype memory chips for the ALICE ITS3 upgrade

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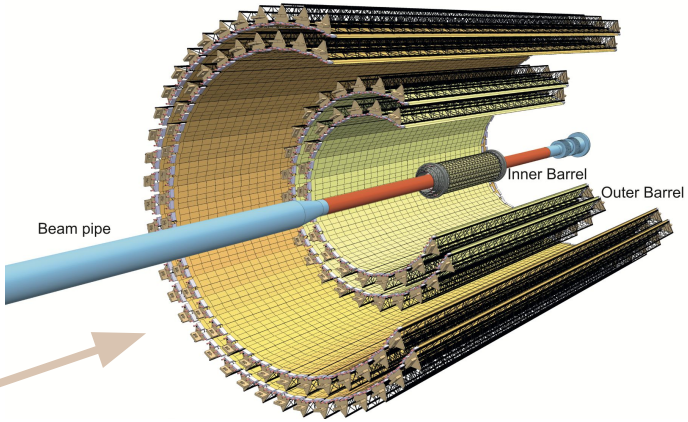
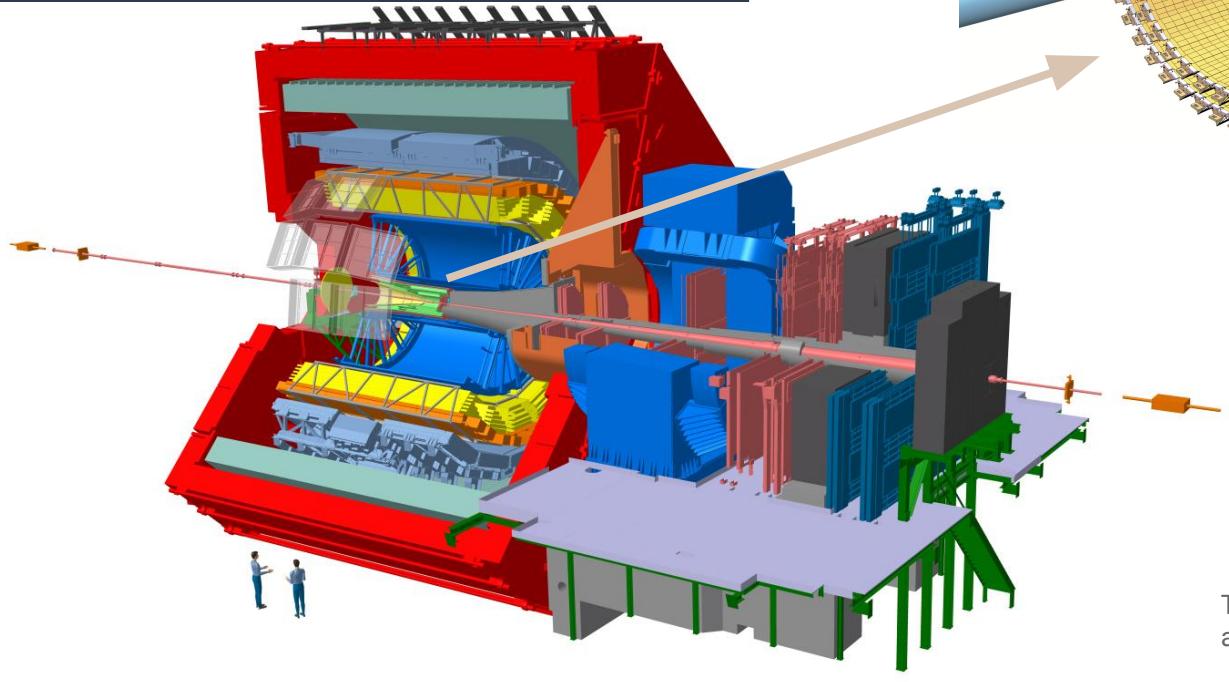
on behalf of the ALICE Collaboration

ALICE

Inner Tracking System of ALICE





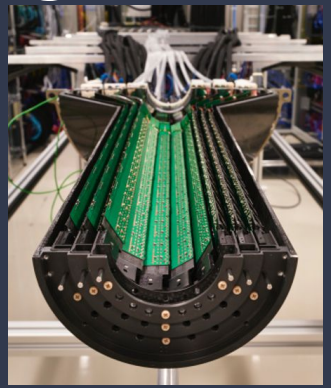
The ALICE experiment schematics (left) and close-up to the ITS2 structure (top).

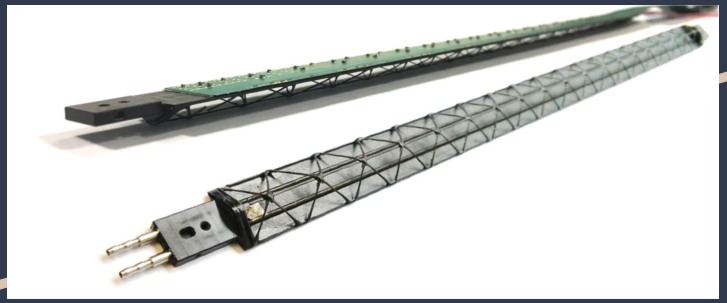
Timea Szollosova (CTU) | Hartmut Hillemans (CERN) | Nicola Minafra (KU)

ALICE ITS upgrade

The inner barrel of the ITS2

- 23 mm from the interaction point
- staves are overlapping

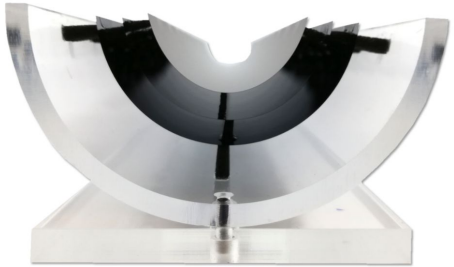




The ITS2 single staves (bottom) and the structure of the ITS2 inner barrel (top) consisting of three layers of partially overlapping staves.

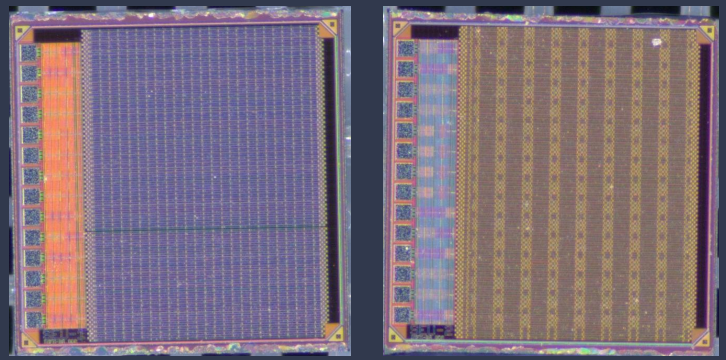
The ITS3 upgrade

- innermost layer only 18 mm away from the IP
- truly bended silicon layers
- carbon foam support
- air cooling



The ITS3 mechanical model (left) of three silicon layers and carbon foam with outside support structure and single layer with readout (right).

Single Event Effects

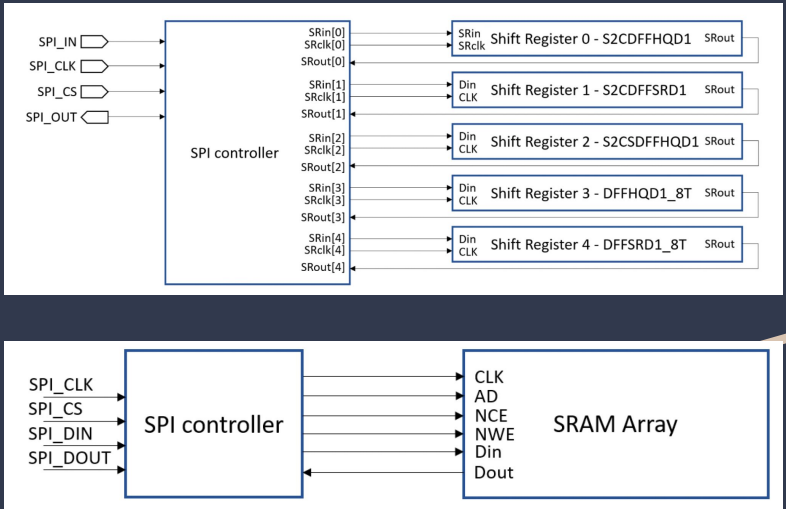


Photos of memory chips designed for SEE measurements.

Studies of reversible single event effects (SEE).

- Single Event Latch-up (SEL)
  - builds parasitic thyristor structure with self sustaining, short circuit like current
  - SEL tests were done using heavy-ions
- Single Event Upset (SEU)
  - charged particle induced bit-flips
  - tests were done using 30 MeV protons from a cyclotron

SEU memory chips



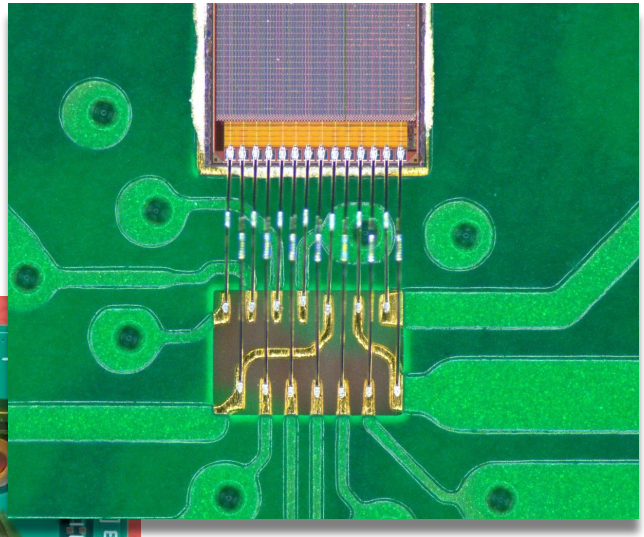
High-level block diagrams of the SEU1 (top) and SEU2 (bottom) chips.

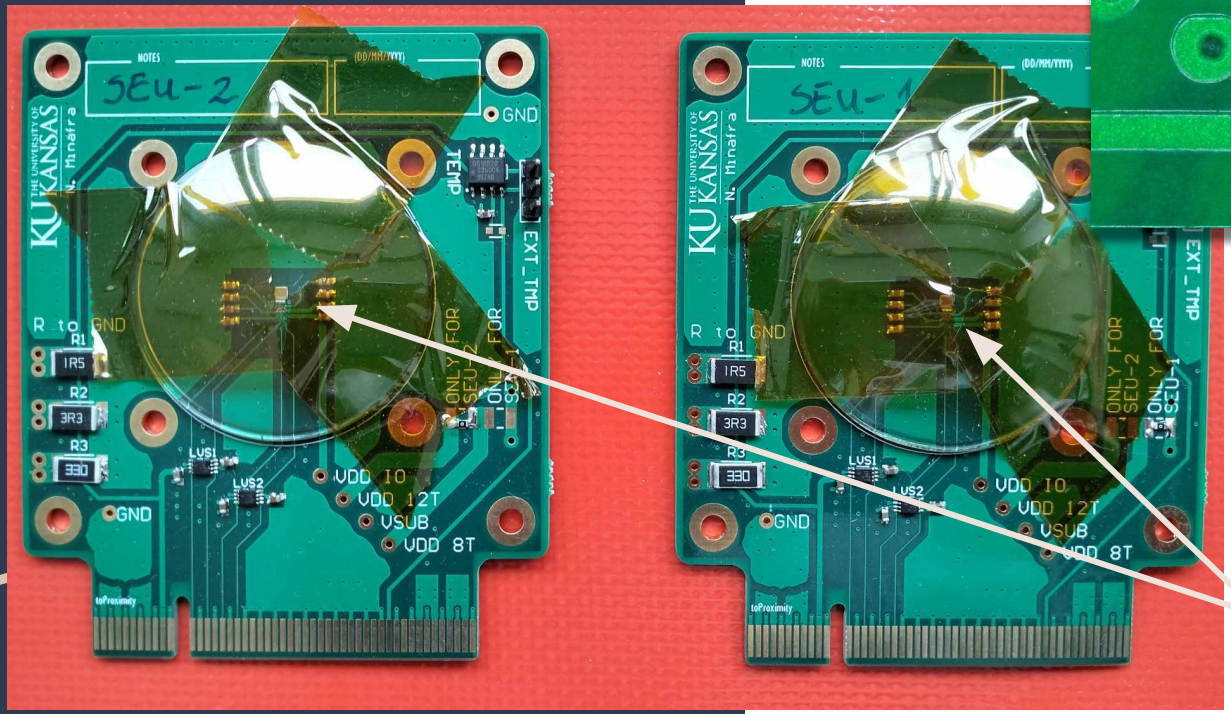
Two dedicated memory chips were designed to study the Single Event Effects sensitivity

Both chips are operated via SPI

- SEU1 consists of FIFO registers:
  - 5 shift registers of 10624 bits
    - 3 from Tower 12 tracks TLV library
    - 2 from CERN compact 8 tracks library
  - 4 power domains
- SEU2 consists of SRAM registers:
  - 128 memory modules, 32 words deep and 16 bits wide
  - 3 power domains

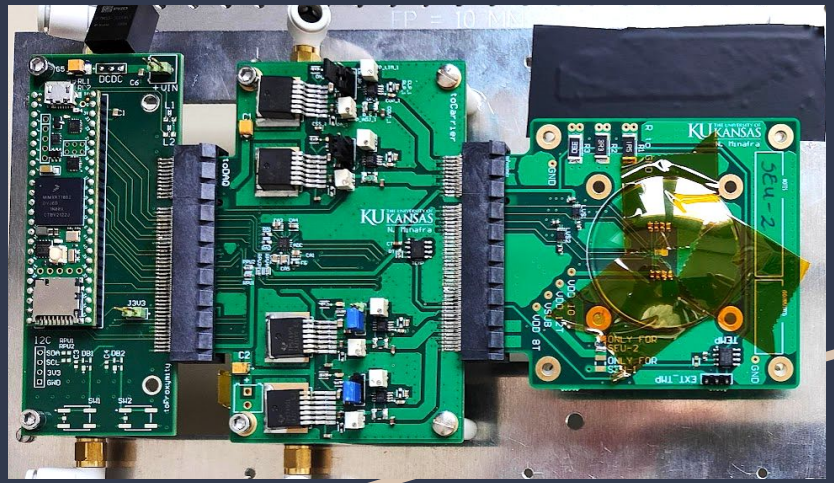
Chips on the boards





The SEU chips (1,5x1,5 mm^2) on boards with protective glass (left) and wire bonding (top).

Tests



Experimental set-up consisting of three carrier boards (Teensy, LDO board, and the chip carrier in this order).

- Teensy microcontroller used for operation and communication with the chip and board monitoring
- memory tests include change and comparison of the pattern stored in the memory
  - SEU1: possibility to exchange the patterns one FIFO at the time as well as all at once
  - SEU2: possibility to just observe the memory without updating the pattern
- SEL: supply current monitoring was implemented for each of the power domains
  - the correct functioning of the chip memory was also being checked during SEL tests
- additional temperature monitoring

SEL tests

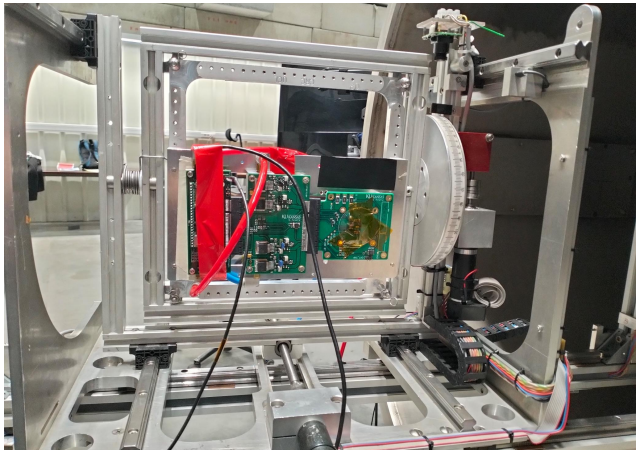
Heavy Ion Facility @UCLouvain (BE)

M/Q	Ion	Energy [MeV]	Range [μm]	LET [MeV/(mg/cm²)]
3,25	$^{13}C^{4+}$	131	269.3	1,3
3,14	$^{22}Ne^{7+}$	238	202,0	3,3
3,37	$^{27}Al^{8+}$	250	131,2	5,7
3,27	$^{36}Ar^{11+}$	353	114,0	9,9
3,31	$^{53}Cr^{16+}$	505	105,5	16,1
3,22	$^{58}Ni^{18+}$	582	100,5	20,4
3,35	$^{84}Kr^{25+}$	769	94,2	32,4
3,32	$^{103}Rh^{31+}$	957	87,3	46,1
3,54	$^{124}Xe^{35+}$	995	73,1	62,5

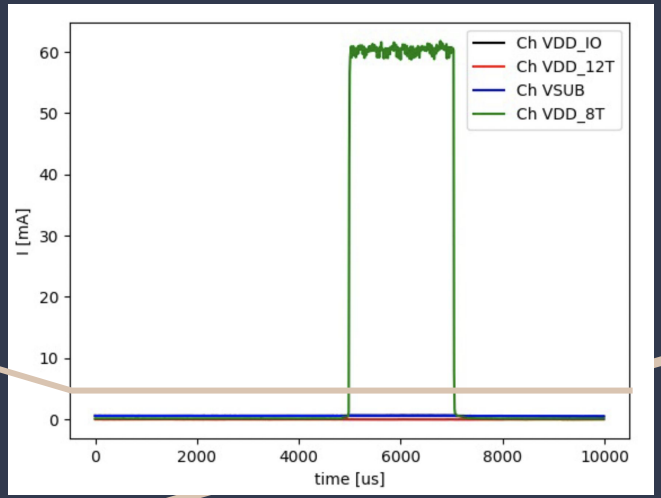
Available particles inside the cocktail with ions used for the tests in green (top) and the vessel for tests (right).

- set-up installed in vacuum vessel
  - connectivity and cooling via vacuum flanges
- heavy-ion fluxes between 500 ions per cm^2 and 15.000 ions per cm^2
- 10% homogeneity over area of 25 mm diameter
- starting from xenon--the highest linear energy transfer--down to argon
- continuous monitoring of supply currents and proper memory functioning

Experimental set-up attached to the holder of the vessel (right).



Results of the SEL tests



5 mA threshold

Current measurements for the SEU1 on all power domains with SEL occurring, producing current of several decades of milliamps.

SEU1

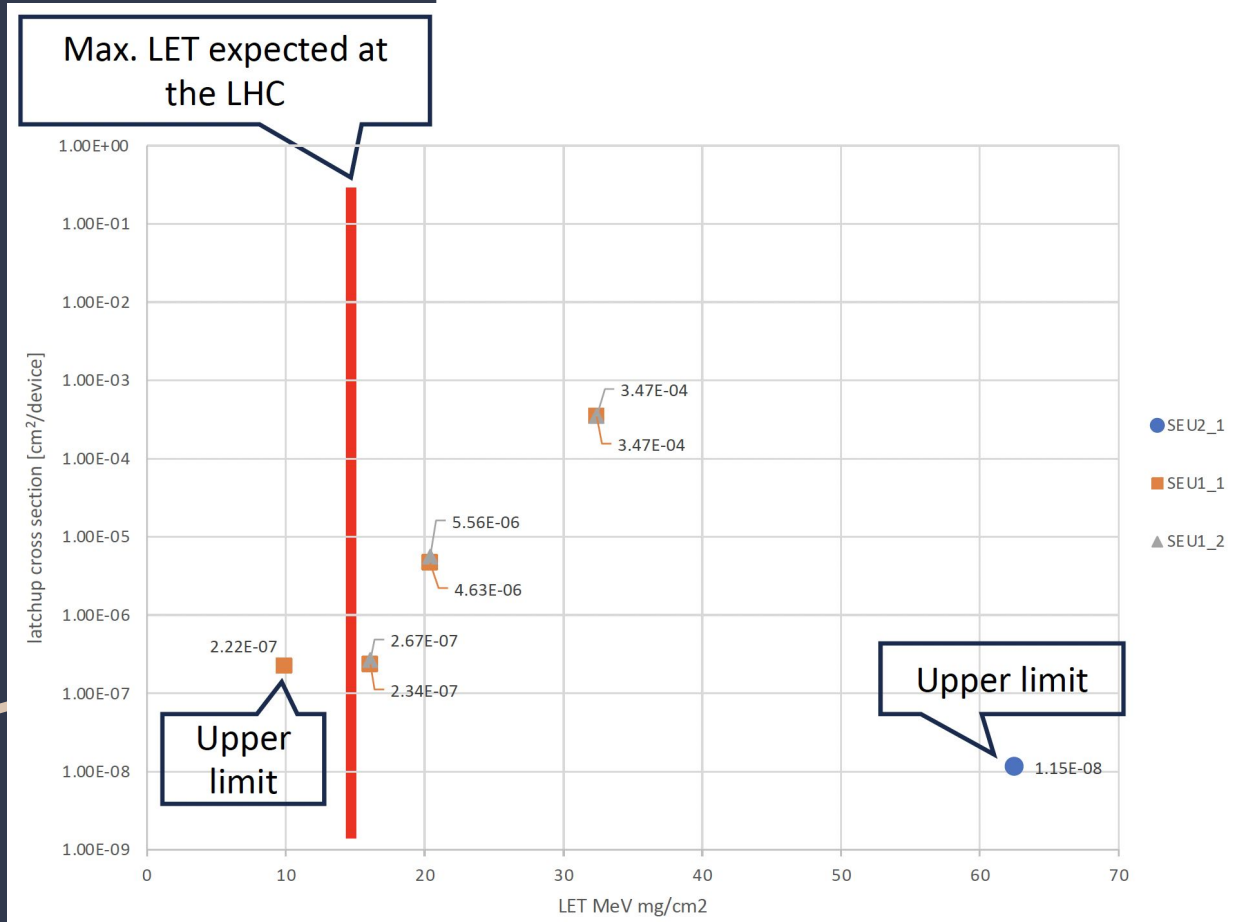
- two prototypes tested
- high latch-up sensitivity for 8T FIFOs
  - for the highest LET (Xe) even at the smallest fluxes (500 ions per cm^2) the measurement was impossible due to instantaneous SEL
  - upper limit at LET = 9.9 MeV/(mg/cm^2) (Ar) after 5 min of no SEL observed
- no latch-ups observed for the 12T FIFOs

SEU2

- one prototype tested
- no latch-ups observed during 3 hours of the highest LET and intensity
- many cross-checks done

Results of the SEL tests

Latch-up cross section with respect to the linear energy transfer of both SEU chips compared with the maximum expected LET for the LHC.



SEU tests reported in this presentation were supported by Ministry of Education, Youth, and Sports of Czech Republic under the award number LM2023040. We also thank the CANAM infrastructure for supporting the tests.

SEU tests

Nuclear Physics Institute @CAS (CZ)

Cyclotron with the set-up installed.

- 24 to 34 MeV/c protons with fluxes from 200 to 10^{12} protons per cm^2/s
- gaussian beam profile has σ of 22 mm
- radiation sensitive electronics was located in a bunker underneath the set-up
- two chips back packed in the beam axis
  - 30 MeV/c on the first and 24 MeV/c on the second according to the GEANT4 simulations
- optimised for achieving one SEU in few seconds
  - fluxes between $4x10^7$ to $2x10^9$ protons per cm^2/s

Experimental set-up attached to the holder - two boards in series.

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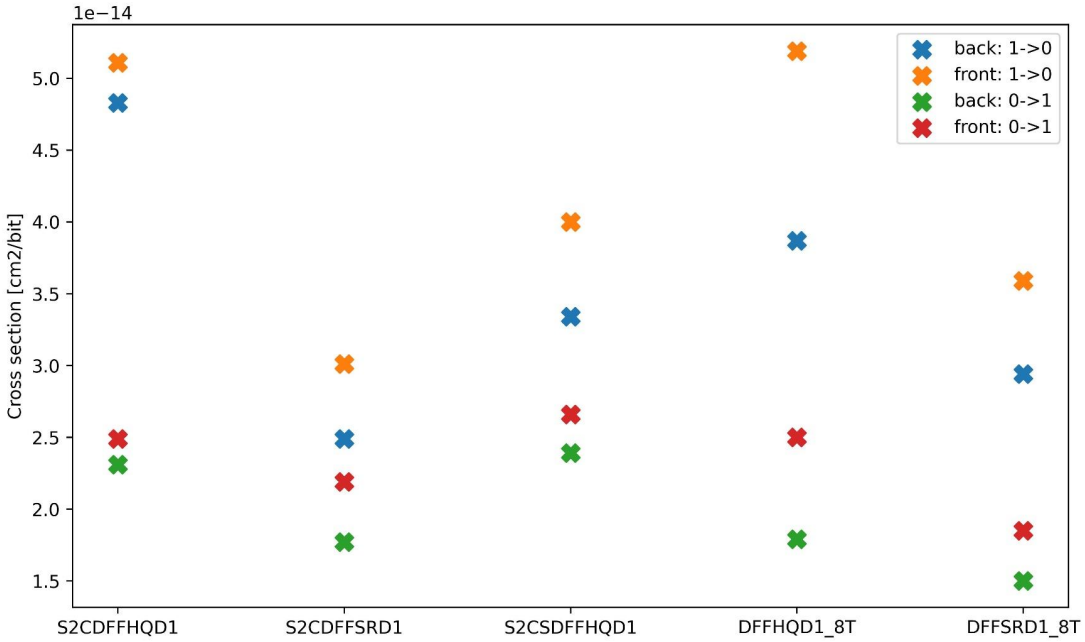
SEU1 results



Cross sections for the each FIFO plotted for different positions (energies) and changes of states. The measurement was done with the flux of 2×10^9 protons per cm^2/s.

The chips were tested at two energies due to simultaneous measurements in series - 30 MeV (first board) and 24 MeV (downstream) (GEANT4).

- asymmetry between 1->0 and 0->1 bit flips for all FIFOs
- significant differences between individual types of FIFO structures
- the cross section for the back chip is smaller

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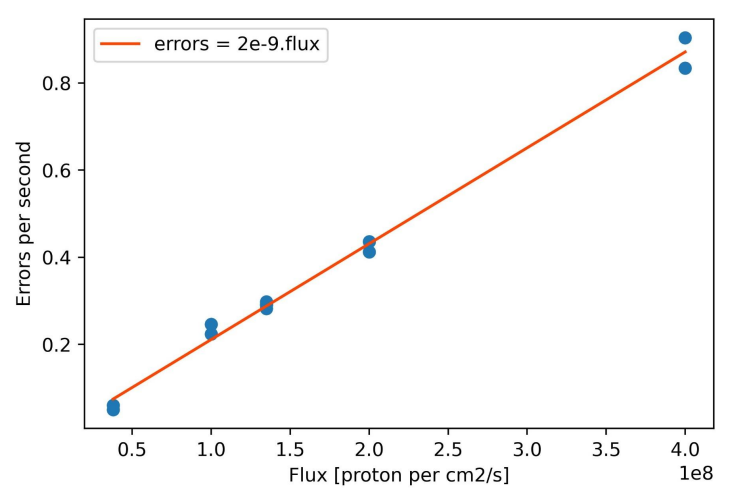
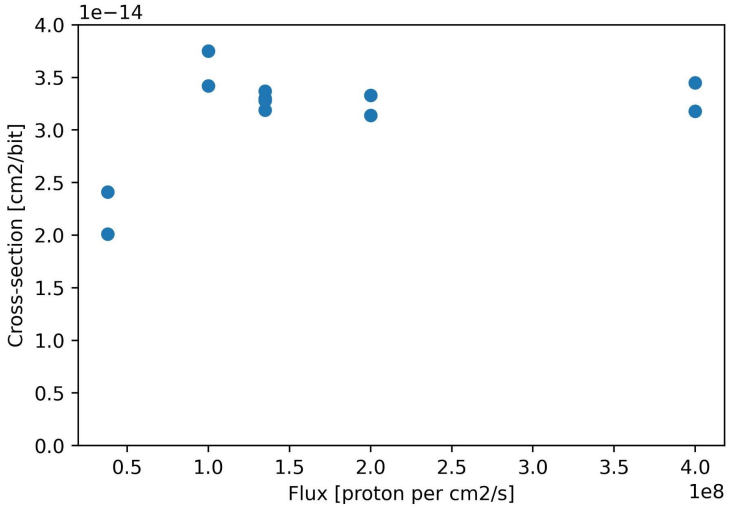
SEU2 results

- no asymmetry between 1->0 and 0->1 observed
- SEU occurrence proportional to the beam flux



Error rate for the SEU2 chip with respect to the beam flux fitted linearly.



Cross section for the SEU2 chip with respect to the beam flux with observable drop for the lowest fluxes, otherwise staying constant.

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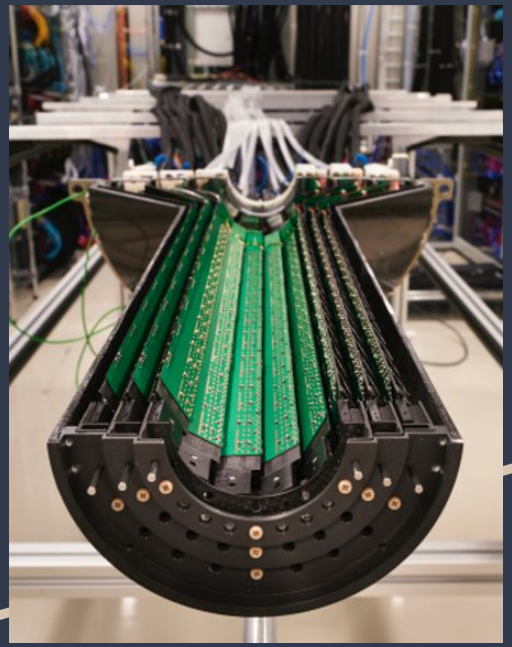
Summary

- the tests of the SEE were done on two SEU memory chips designed for this purpose
- SEL
  - only the 8T FIFO is sensitive
  - no latch-ups below the maximum expected LHC LETs were observed
- SEU
  - the cross section were in orders of 3 to 5×10^{-14} cm^2/bit for all types of memory
  - the results are comparable to previous tests
- future tests within the ITS3 sensor developments are done using larger prototype sensors

Thank you!

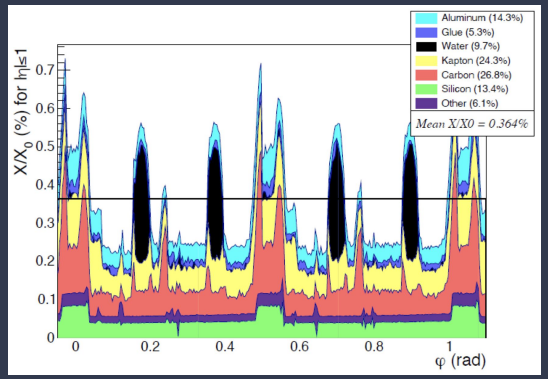
Backup

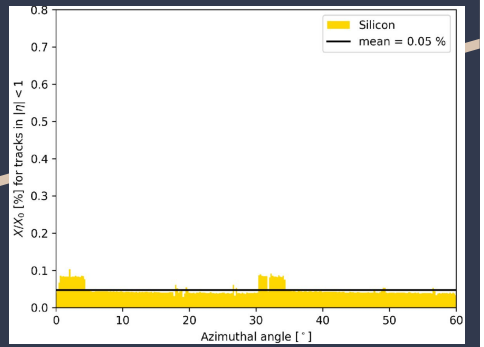
ITS2



- 23 mm from the interaction point
- consists of three parts:
  - space frame = support stucture
  - cold plate = thermal-conductive carbon fibre with embedded polyamide cooling pipes
  - Hybrid Integrated Circuit = Flexible Printed Circut with Pixel Chips bonded onto it
- adjacent staves are partially overlapping

ITS3





Azimuthal distribution (averaged over the full barrel length) of the material budget of the Layer 0 for the current ITS2 (top) and the future ITS3 (right).

- 18 mm for the IP
- pure silicon
  - 20 - 40 μm thickness
  - dimensions of the whole stave
- carbon foam
- air cooling
- significant cost reduction